

PCB NO : DAA0000J000

BOM P/N :

ZZZ
DAA0000J010
PCBR1@
PCB 3JJ LA-K454P REV1 MB

ZZZ
DAA0000J011
PCBR3@
PCB 3JJ LA-K454P REV1 MB GOLD A31 !

ZZZ
DAA0000J012
PCBR3@
PCB 3JJ LA-K454P REV1 MB TRIPOD A31 !

ZZZ
DAA0000J013
PCBR3@
PCB 3JJ LA-K454P REV1 MB HANNSTARB A31 !

PCB

ZZZ
DAA0000J000
PCB@
PCB 36M LA-K454P REV0 MB S

Compal Confidential

FP6 Cezanne-H GN20P MB Schematic Document

Rev: 1.0

2021.04.21

@ : Un-pop Component

EMI@/ESD@/RF@ : EMI, ESD and RF Component

@EMI@/@ESD@/@EMC@ : EMI, ESD and RF Un-POP Component

PCB@/PCBR1@/PCBR3@ : MB PCB Partnumber

ARK@/SIF@ : ARK or SIF sku

TYPEC@ : Type-C

N18P@/N20P@ : option with N18P or N20P

45492@/45495@ : 45492 for N18P 45495 for N20P

CONN@ : Connector Component

EVT@/DVT1@/DVT2@/PVT@ : Build Phase

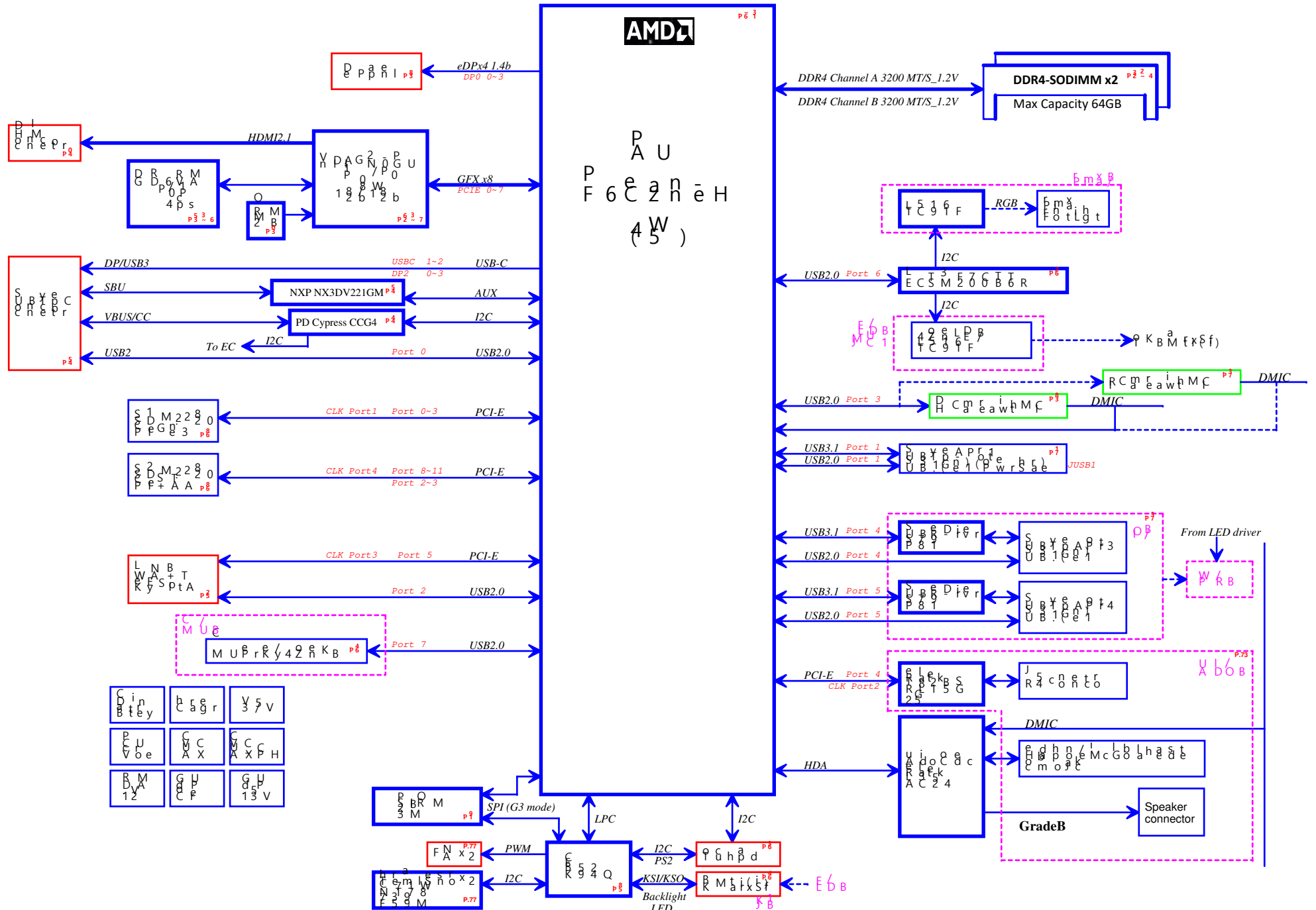
GN20P0@/GN20P1@/GN20P0D@ : GPU

GC6@ : GC6 function for GPU

X76S@/X76M@/X76H@ : VRAM option

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Block Diagram



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Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)								
S3 (Suspend to RAM)								
S4 (Suspend to Disk)								
S5 (Soft OFF)								

PCH SMBUS Address Table

PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK	+3VALW_PCH	JDIMM1	
PCH_SMBDATA		JDIMM2	

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS		
		Thermal 1	0x98h
		Thermal 2	0x9Ah
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	BAT	TBD
		CHGR	TBD
DAT_TP_SIO_I2C_CLK CLK_TP_SIO_I2C_DAT	+TP_VDD	Touch Pad	TBD
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG5C	0x08

Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	EVT@
1	DVT1@
2	DVT2@
3	PVT@
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

GPU ID Table

GPU ID	
0	GN20E3@
1	GN20E4@
2	GN20E5@
3	GN20E7@
4	GN20P0@
5	GN20P1@
6	GN20P0D@
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

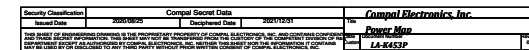
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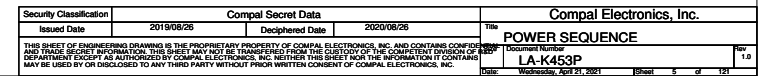
Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN						
+12.6V_BATT+						
+19VB						
+VCC_CORE						
+VCCGT						
+VCCSA						
+VCCIO						
+3.3V_BAT_LDO						
+RTC_CELL						
+5VALW						
+3VALW						
+3VALW_PCH						
+3VALW_DSW						
+1.8V_PRIM						
+1VALW						
+1.2V_DDR						
+0.6V_DDR_VTT						
+2.5V_MEM						
+VCCST						
+VCCSTG						
+5VS						
+3VS						
+1.8VS						

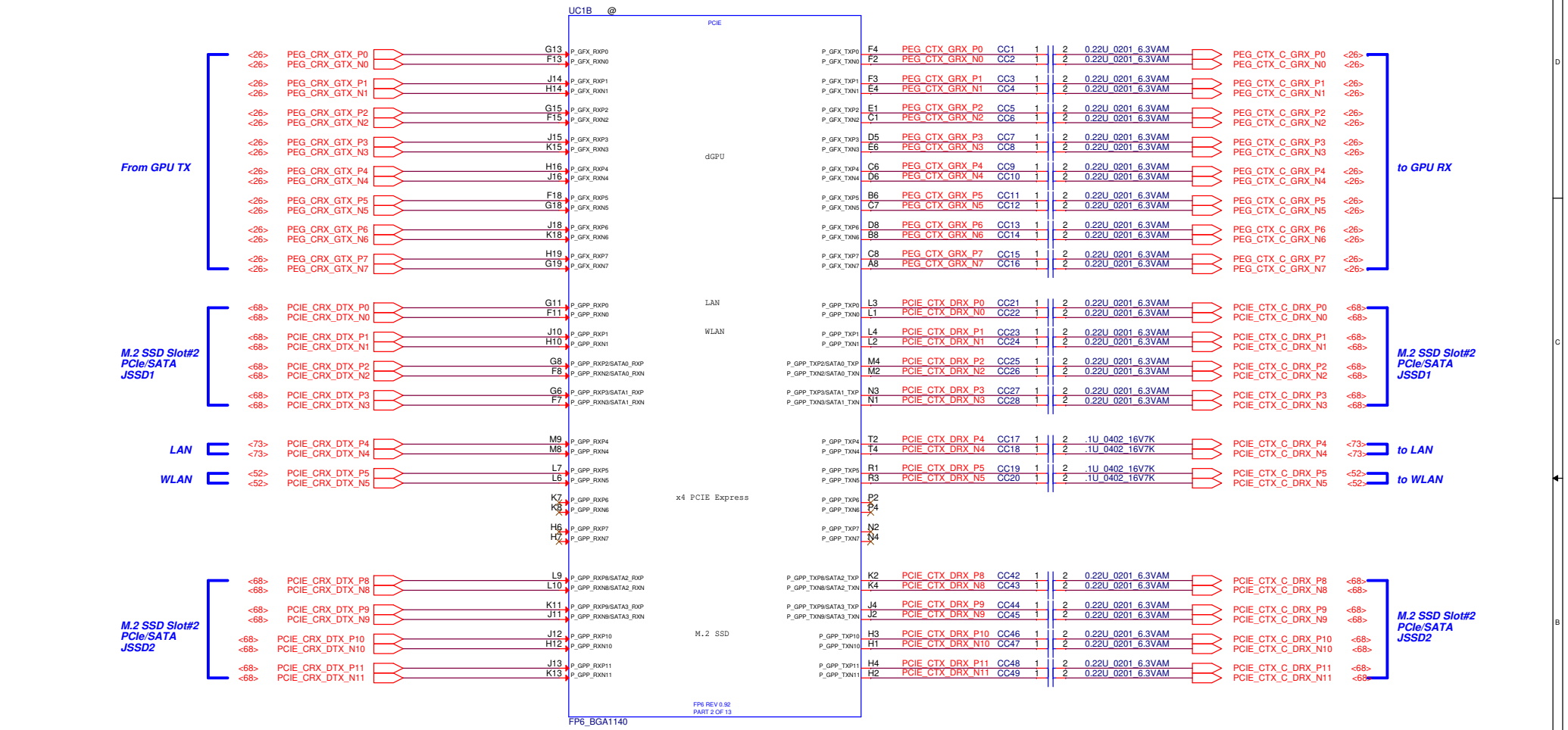
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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Main Func = CPU



APU PN Table

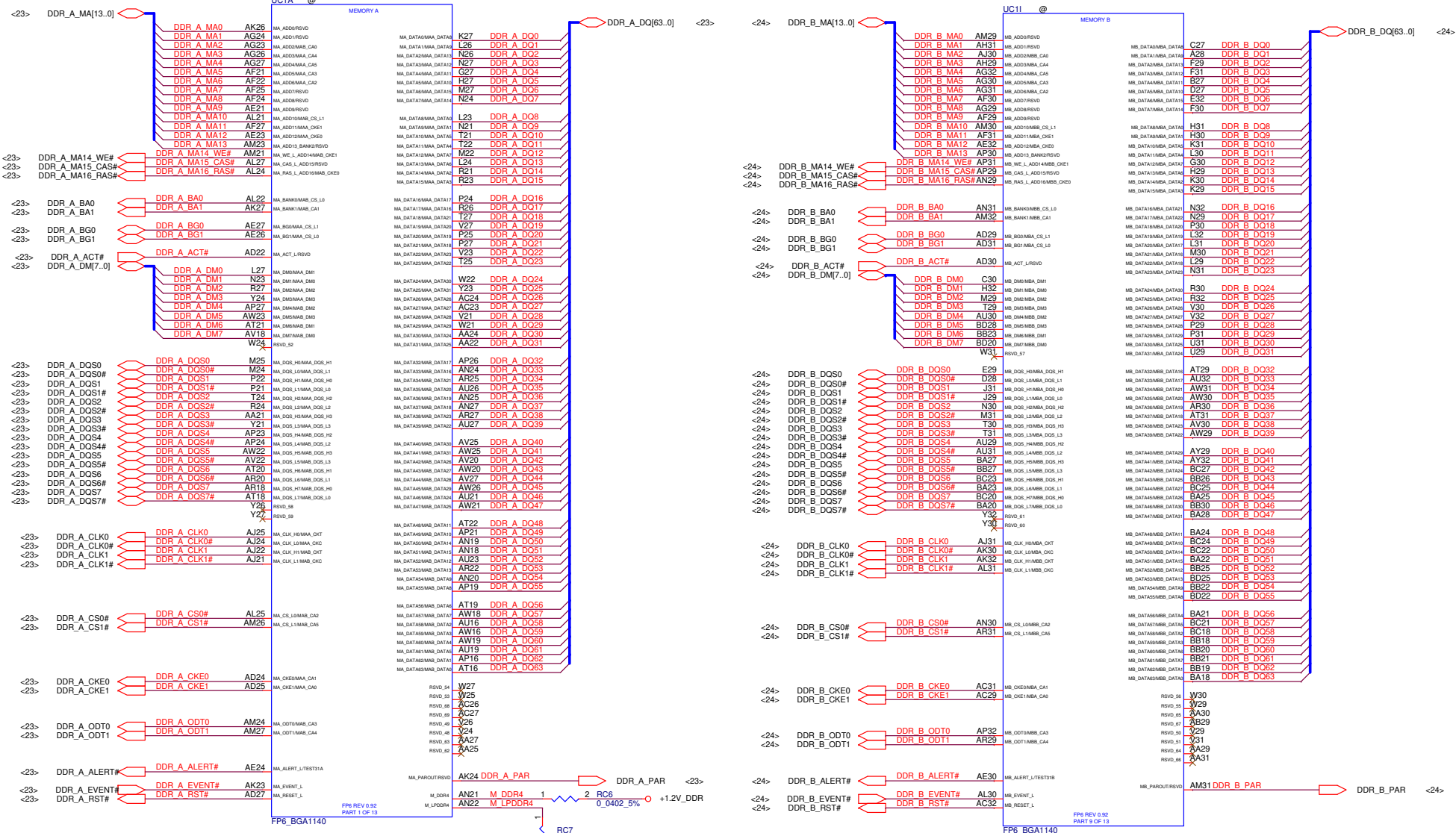
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UC1	S IC RYZEN7 100-000000295 3.2G APU A31! R7@ SA0000E1P3L
UC1	S IC RYZEN9 100-000000300 3.3G APU A31! R9@ SA0000E1N3L

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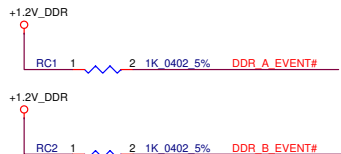
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		Rev	1.0

Main Func = CPU

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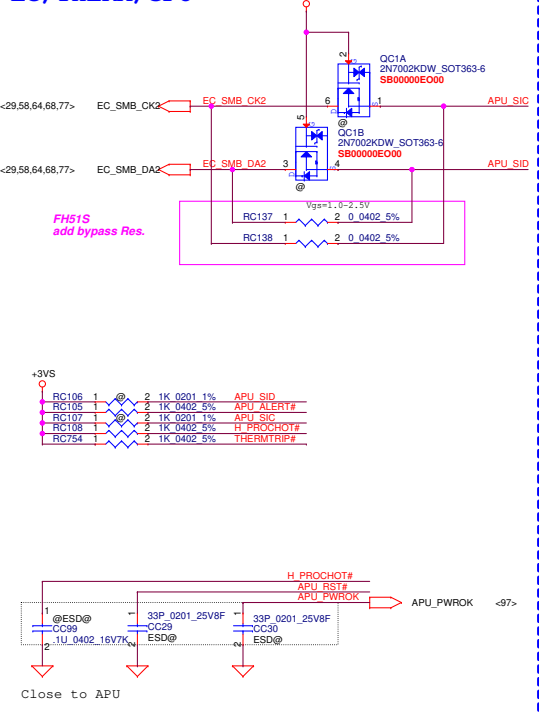
EVENT# pull high



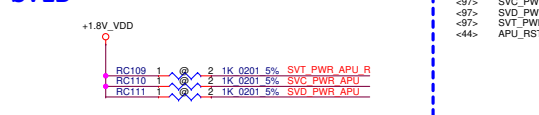
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				Document Number		LA-K453P	
Date: Wednesday, April 21, 2021				Sheet 7 of 121			

Main Func = CPU

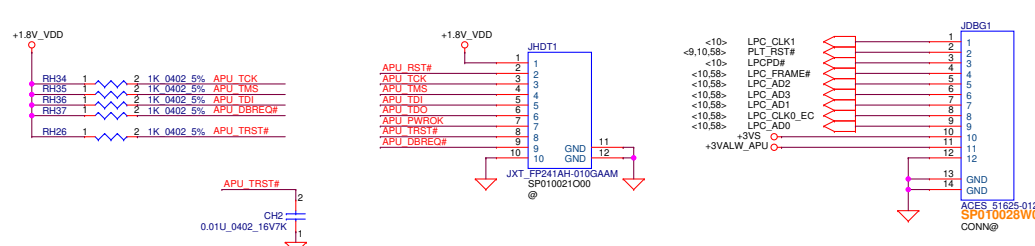
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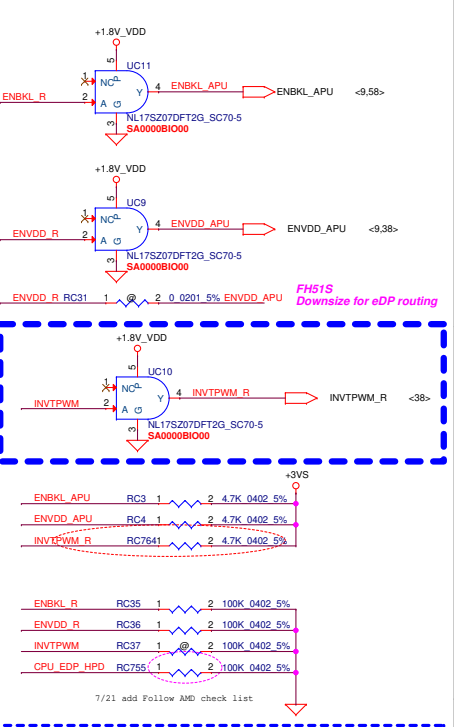
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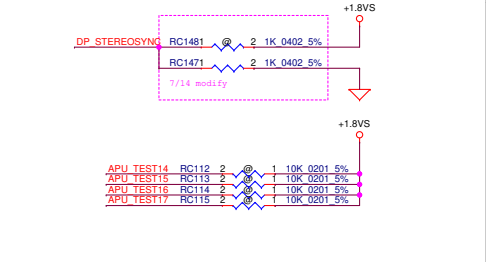
AMD DEBUG



DISP

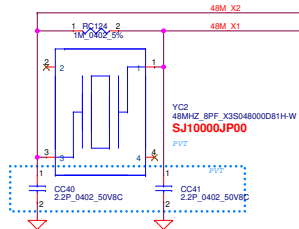


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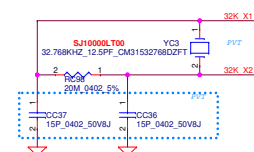


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				FP6 (3/7) DISP/MISC/HDT	
				Document Number	
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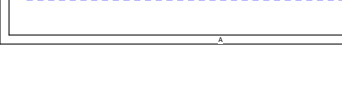
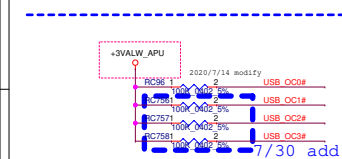
48MHz CRYSTAL



32.768KHz CRYSTAL



USB Function



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<71> USB20_N2 << A05

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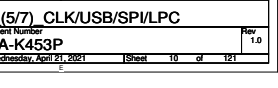
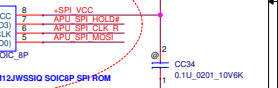
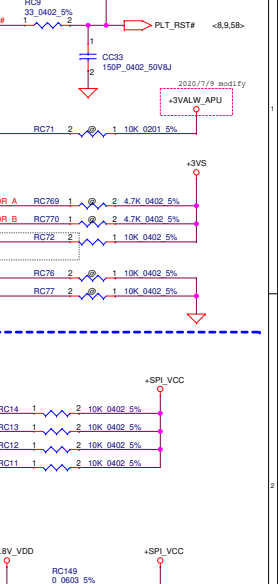
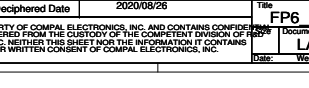
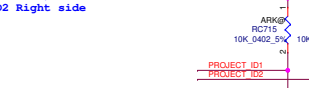
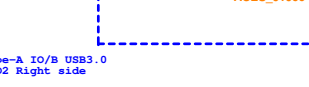
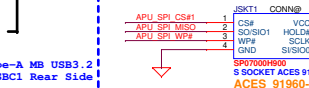
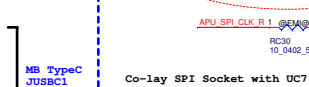
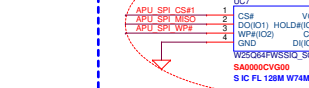
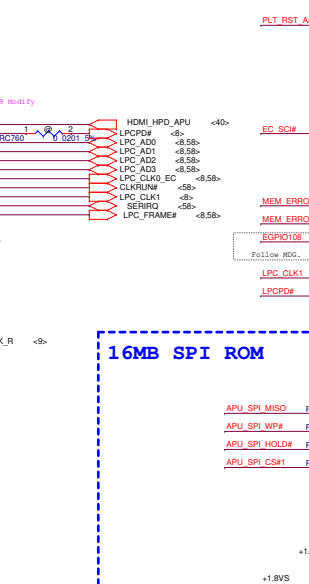
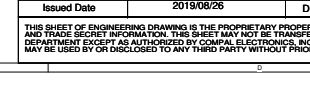
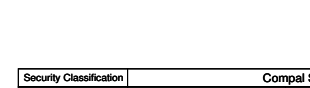
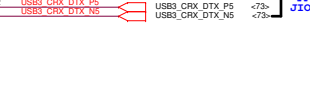
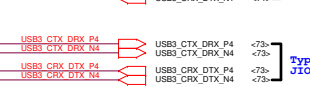
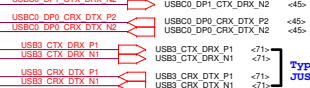
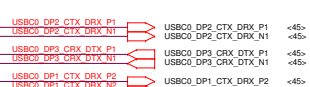
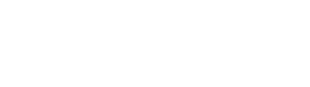
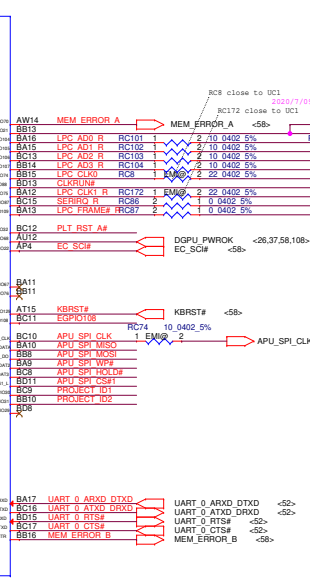
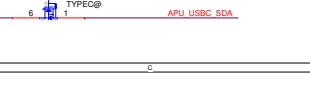
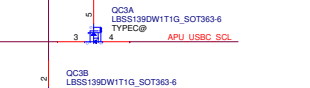
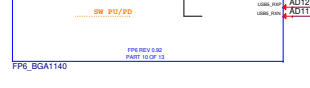
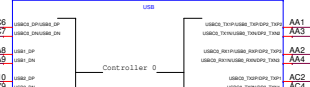
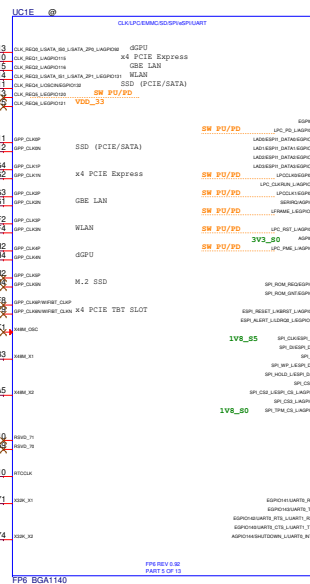
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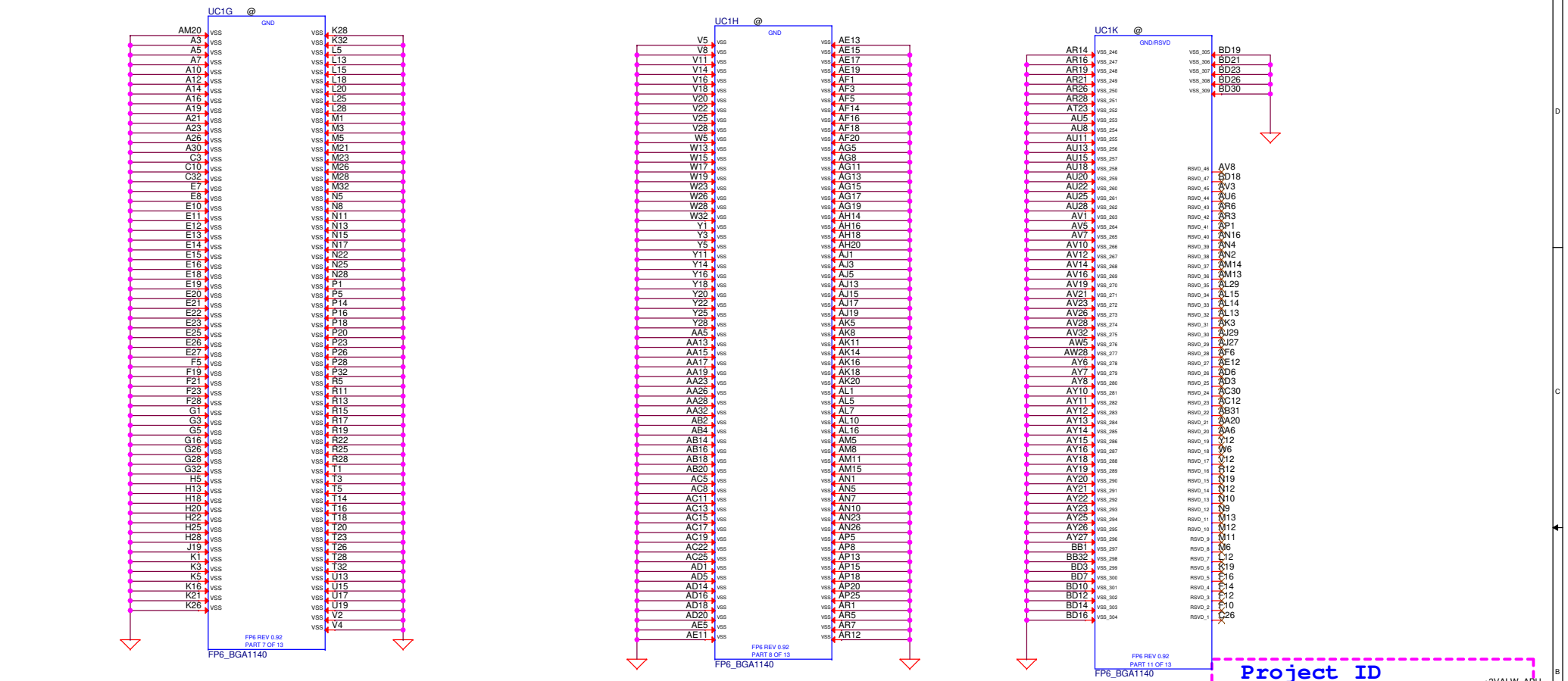
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Main Func = CPU



Project ID

+3VALV ARU

GPUID 100K 0201 5% 2 N20E@ 1 RC169

GPUID 100K 0201 5% 1 N20P@ 2 RC171

Pin Name	SIF / ARK
SIF	LOW SIF@
ARK	HIGH ARK@

N20E / N20P

GPUID	NV - GN20P	LOW N20P@
	NV - GN20E	HIGH N20E@

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								LA-K453P		1.0	
								Date:		Wednesday, April 21, 2021	

Reserve

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Reserve

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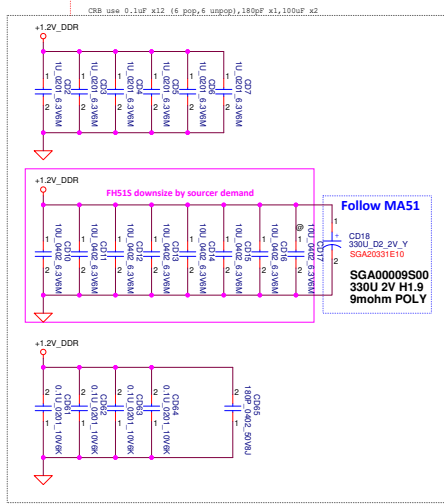
Interleaved Memory

REVERSE TYPE (4 mm)

Layout Note: Place near JDIMM1	Note: Check voltage tolerance of VREF_DQ at the DIMM socket
-----------------------------------	---

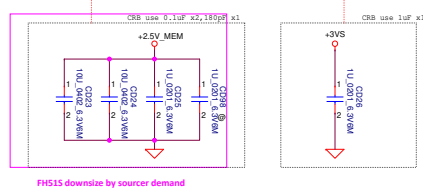
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Check voltage tolerance of
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DDR4 support Even Parity check in DRAMs.

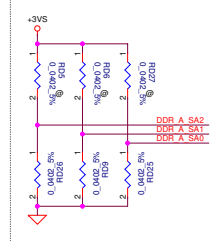


Layout Note:
Place near JDIMM1.257,259

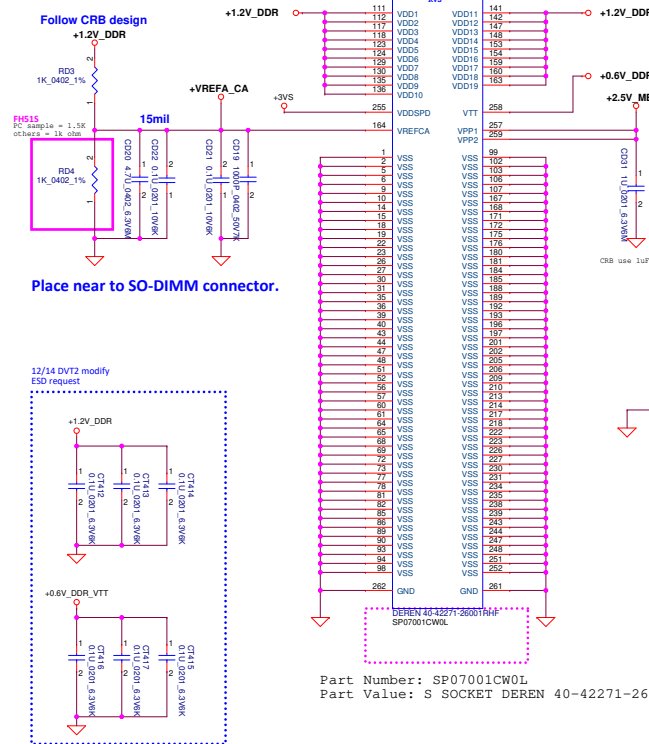
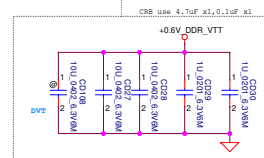
Layout Note:
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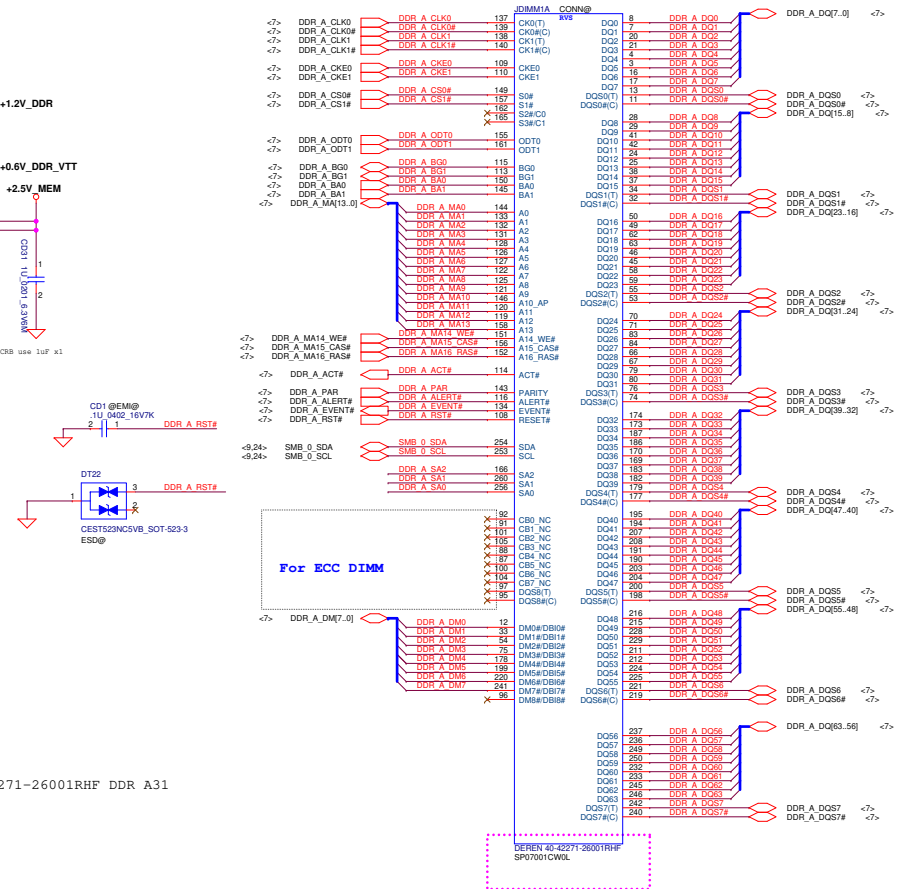
Address : A0



Layout Note:
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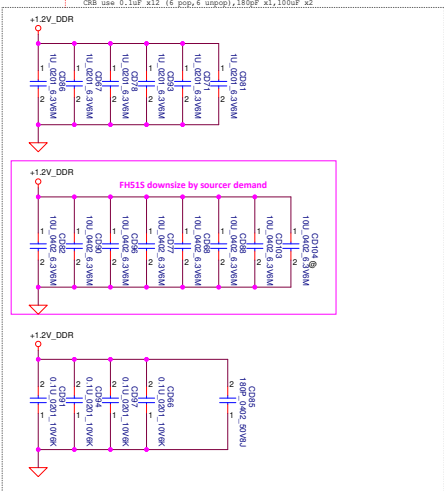
Part Number: SP07001CW0L
Part Value: S SOCKET DEREN 40-42271-26001RHF DDR A31



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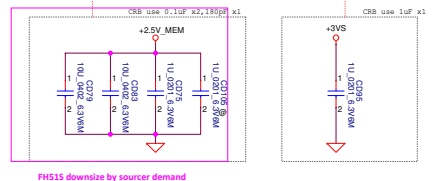
Layout Note: Place near JDIMM2	Note: Check voltage tolerance of VREF DQ at the DIMM socket
-----------------------------------	---

Note:
Check voltage tolerance of
VREF D0 at the DIMM socket

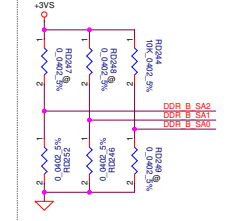


Layout Note:
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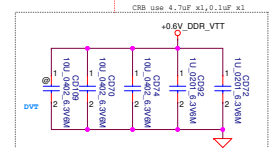
Layout Note:
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Address : A2



Layout Note:
Place near JDTMM2 258



Part Number: SP07001GK0L
Part Value: S SOCKET DEREN 40-42261-26001RHF A31

Layout Note:
Place near JDIMM2 258

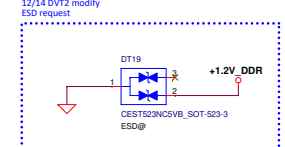
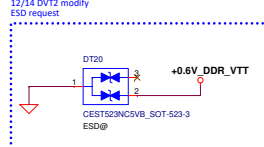
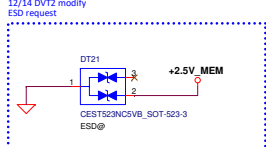
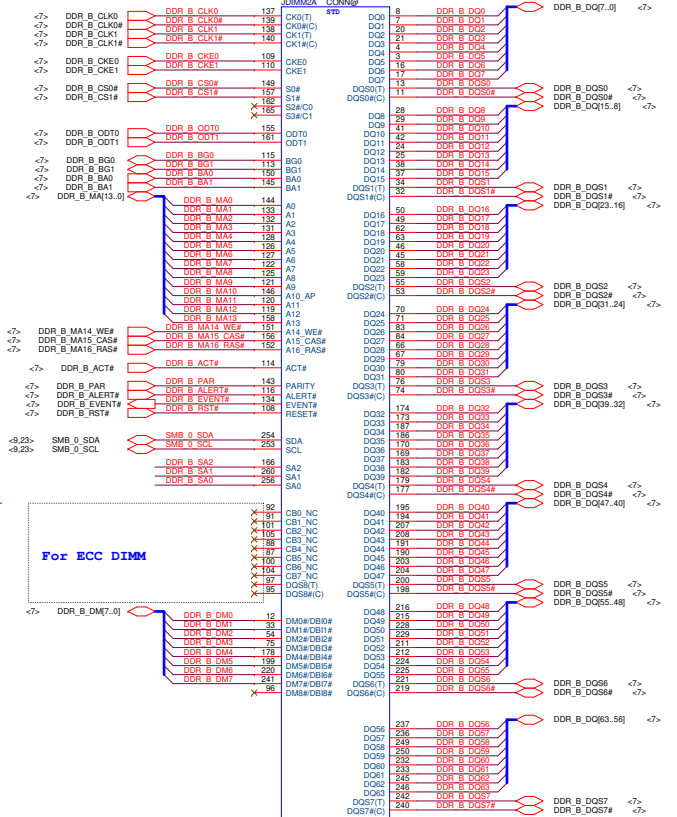
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***** CRS use 4.7uF x1,0.1uF x1 *****
```

[illegible]

Interleaved Memory
















STD (4 mm)

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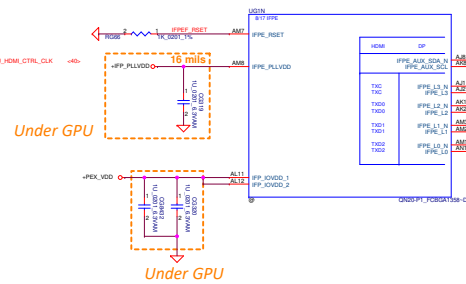
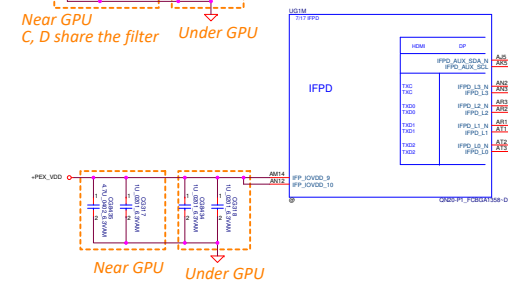
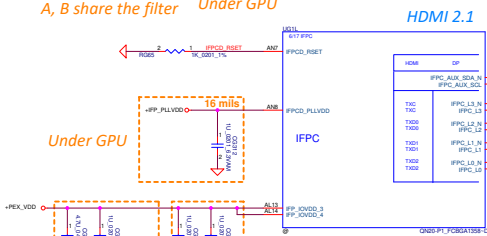
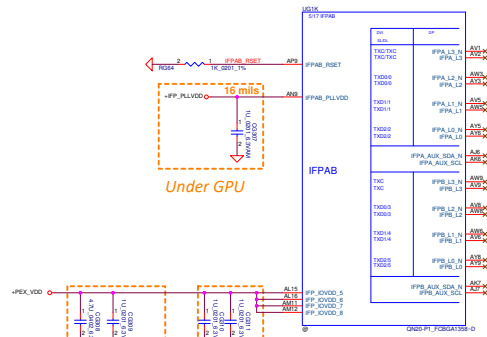


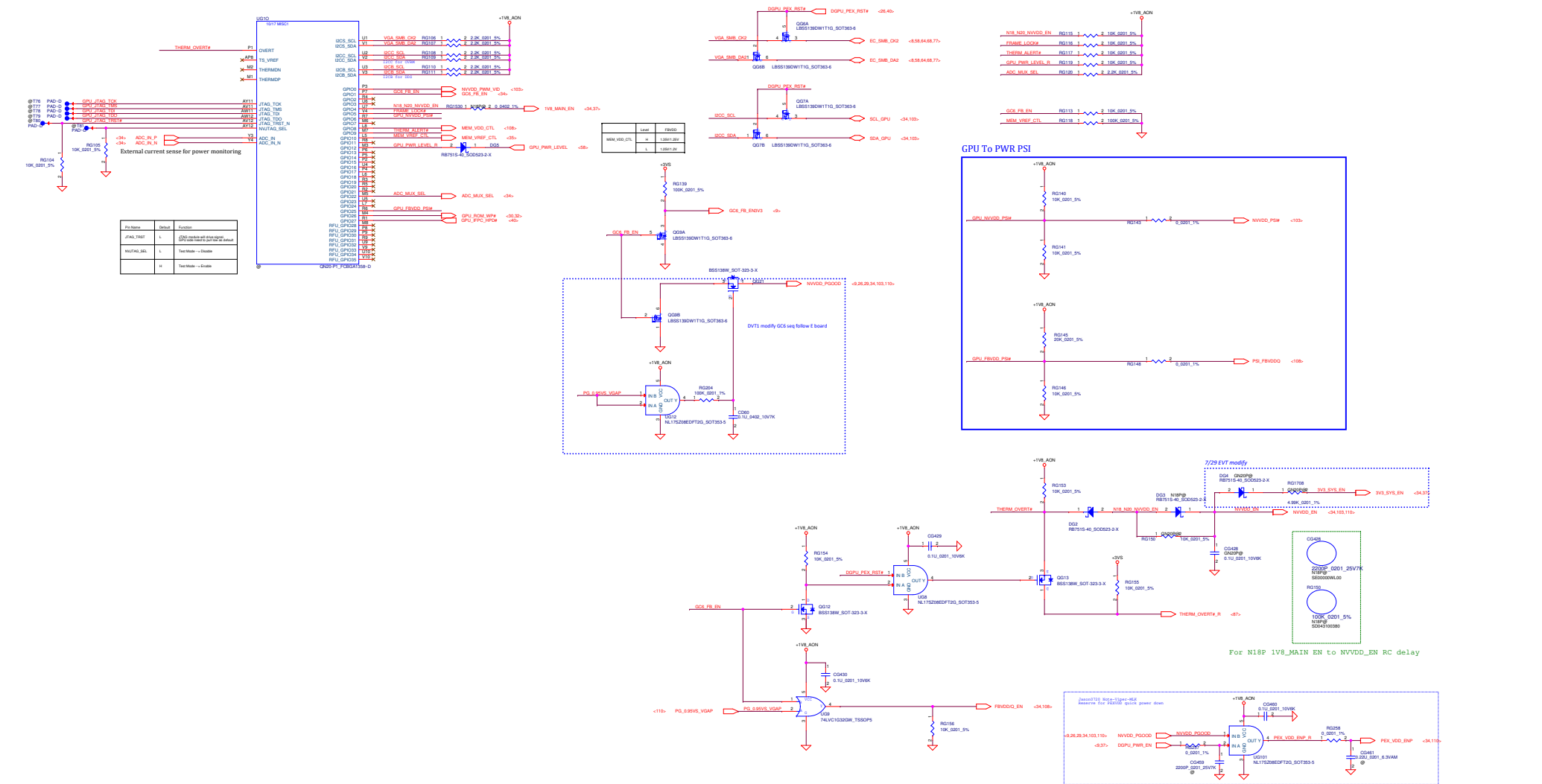
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Main Function:

VRAM Configuration			
Samsung	Hynix	Micron	X76
<div>UM9 SAM@</div> <div></div> <div>K4Z80325BC-HC14 1.2V SA0000C626L</div>	<div>UM9 HYNIX@</div> <div></div> <div>H56C8H24AIR-S2C FBGA 180P SA0000DUW1L</div>	<div>UM9 MIC@</div> <div></div> <div>MT61K256M32JE-14:A1.2V SA0000BND7L</div>	<div>ZZZ3 X76S@</div> <div></div> <div>ALT. GROUP PARTS VRAM 4G SAM X7691031L61</div>
<div>UM10 SAM@</div> <div></div> <div>K4Z80325BC-HC14 1.2V SA0000C626L</div>	<div>UM10 HYNIX@</div> <div></div> <div>H56C8H24AIR-S2C FBGA 180P SA0000DUW1L</div>	<div>UM10 MIC@</div> <div></div> <div>MT61K256M32JE-14:A1.2V SA0000BND7L</div>	<div>ZZZ1 X76H@</div> <div></div> <div>ALT. GROUP PARTS VRAM 4G HYN X7691031L63</div>
<div>UM11 SAM@</div> <div></div> <div>K4Z80325BC-HC14 1.2V SA0000C626L</div>	<div>UM11 HYNIX@</div> <div></div> <div>H56C8H24AIR-S2C FBGA 180P SA0000DUW1L</div>	<div>UM11 MIC@</div> <div></div> <div>MT61K256M32JE-14:A1.2V SA0000BND7L</div>	<div>ZZZ2 X76M@</div> <div></div> <div>ALT. GROUP PARTS VRAM 4G MIC X7691031L62</div>
<div>UM12 SAM@</div> <div></div> <div>K4Z80325BC-HC14 1.2V SA0000C626L</div>	<div>UM12 HYNIX@</div> <div></div> <div>H56C8H24AIR-S2C FBGA 180P SA0000DUW1L</div>	<div>UM12 MIC@</div> <div></div> <div>MT61K256M32JE-14:A1.2V SA0000BND7L</div>	

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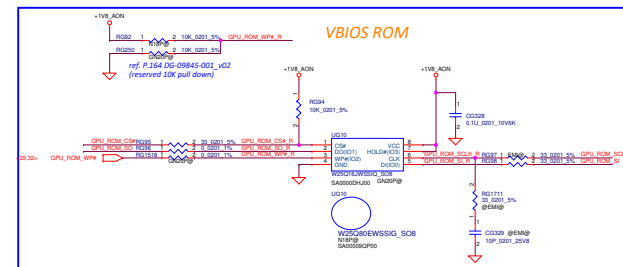
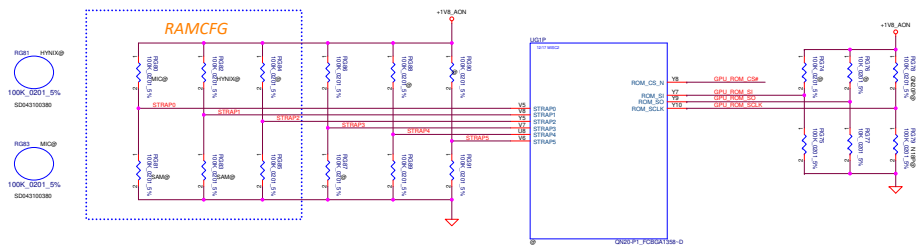


Table 9.3 RAMCFG

Strap Pins <small>See Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	<small>(see Memory RVL for memory configs corresponding to these numbers)</small>
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)

Table 4. GN20-P1/P0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
8 Gb	2Chx256Mx16	1.25V and 1.2V ¹	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ²	Full	Production candidate	ES or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	Qs1 or later
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 ³	Full	Production candidate	Qs2 or later

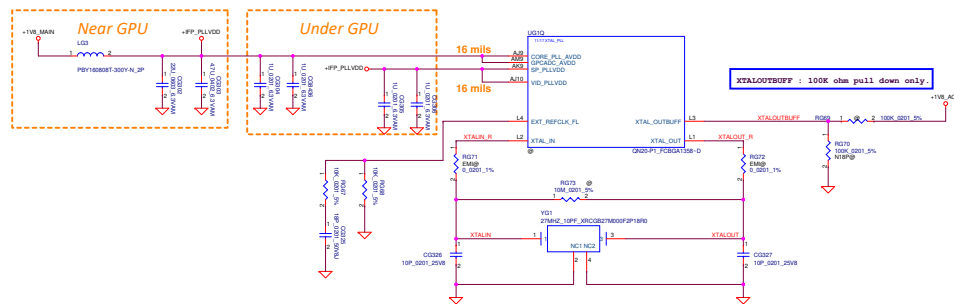
Notes:

¹ DVS is required to run WCLK > 5500 MHz.

² Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SP" letters inserted before the seven digits in its lot ID.

³ Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.

For GN20-P1/P0, the maximum allowable memory case temperature is 95 °C.



STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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LA-R662P		

UG1E

1617 QND.1.2

A10

GND

001

A2

GND

001

A25

GND

002

A31

GND

003

A34

GND

004

A37

GND

005

A39

GND

006

A4

GND

007

A41

GND

008

AB13

GND

009

AB14

GND

010

AB15

GND

011

AB16

GND

012

AB17

GND

013

AB18

GND

014

AB19

GND

015

AB30

GND

016

AB31

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017

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042

AE31

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044

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AH10

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AH11

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AH12

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063

AH13

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064

AH16

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065

AH17

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AH28

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AH32

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079

AH34

GND

080

AH35

GND

081

AH4

GND

082

AH6

GND

083

AH8

GND

084

AJ3

GND

085

AJ32

GND

086

AJ34

GND

087

AJ35

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088

AJ36

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AK10

GND

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AK11

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AK36

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AL4

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AL40

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AL6

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AM15

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AM29

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AN4

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AP12

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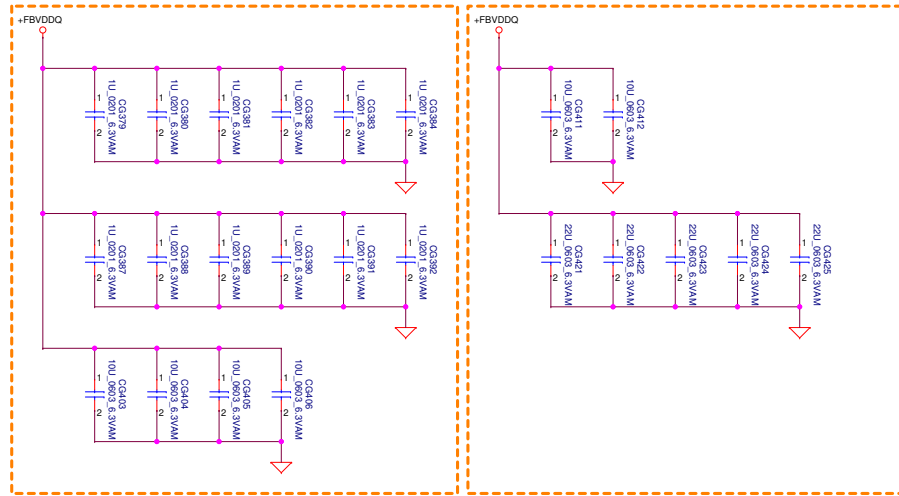
448

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title	NV(6/8) GND, RFUs
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FBVDDQ_GPU

Under GPU

Near GPU



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				LA-K662P	
Date:				Wednesday, April 21, 2021	Sheet 33 of 121

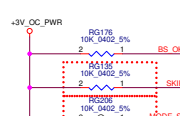
OVRM Gen1 with N18P-G61-A



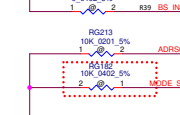
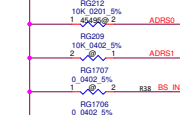
OVRM Gen2 with GN20P/P1



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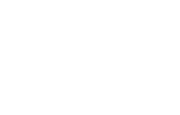
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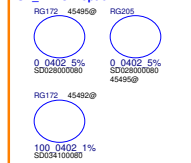
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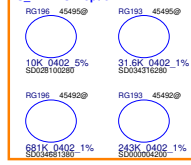
SH_O BOM option



SH_IN BOM option



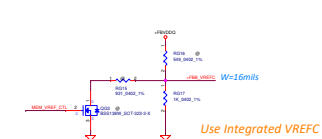
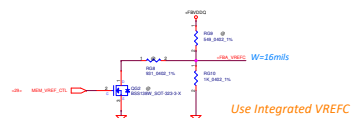
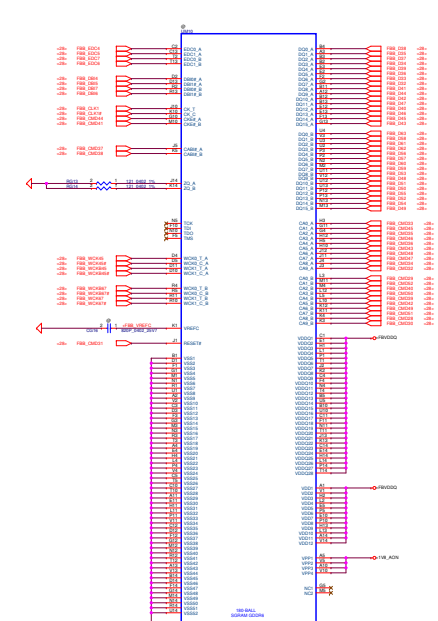
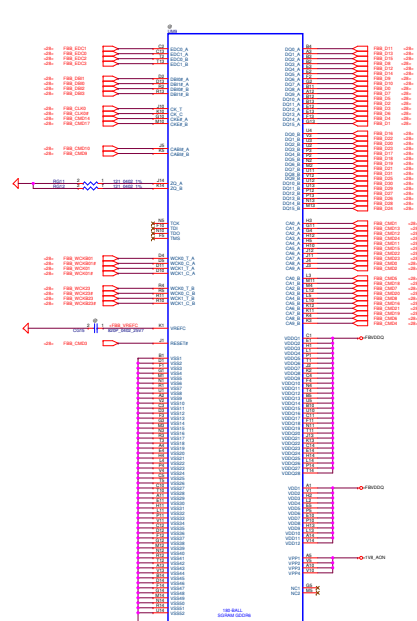
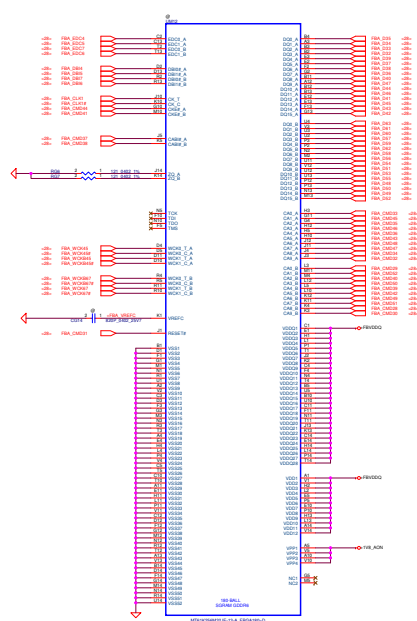
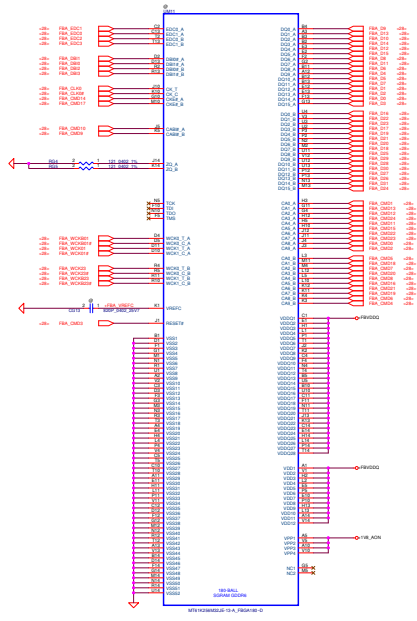
BS_REF BOM option



BS_IN BOM option



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Doc No: LA-K662P				Date: Wednesday, April 21, 2021	Sheet 34 of 121

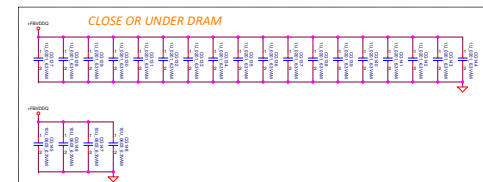
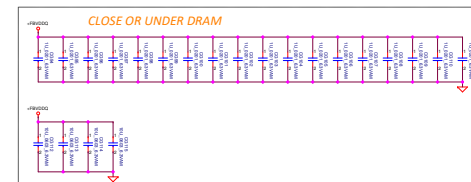
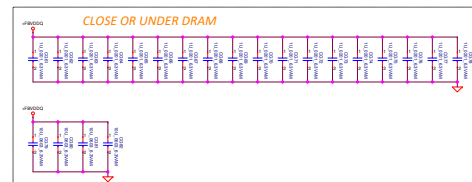
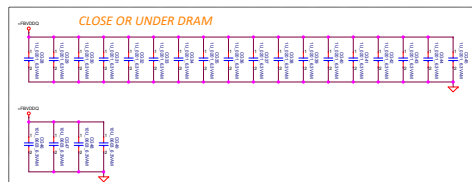
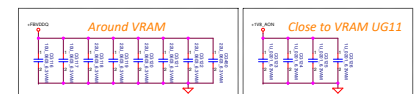
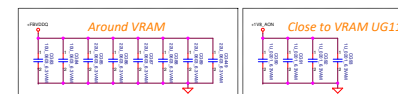
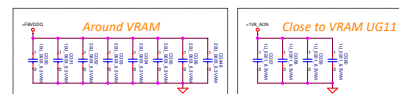
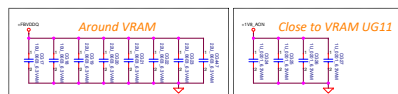


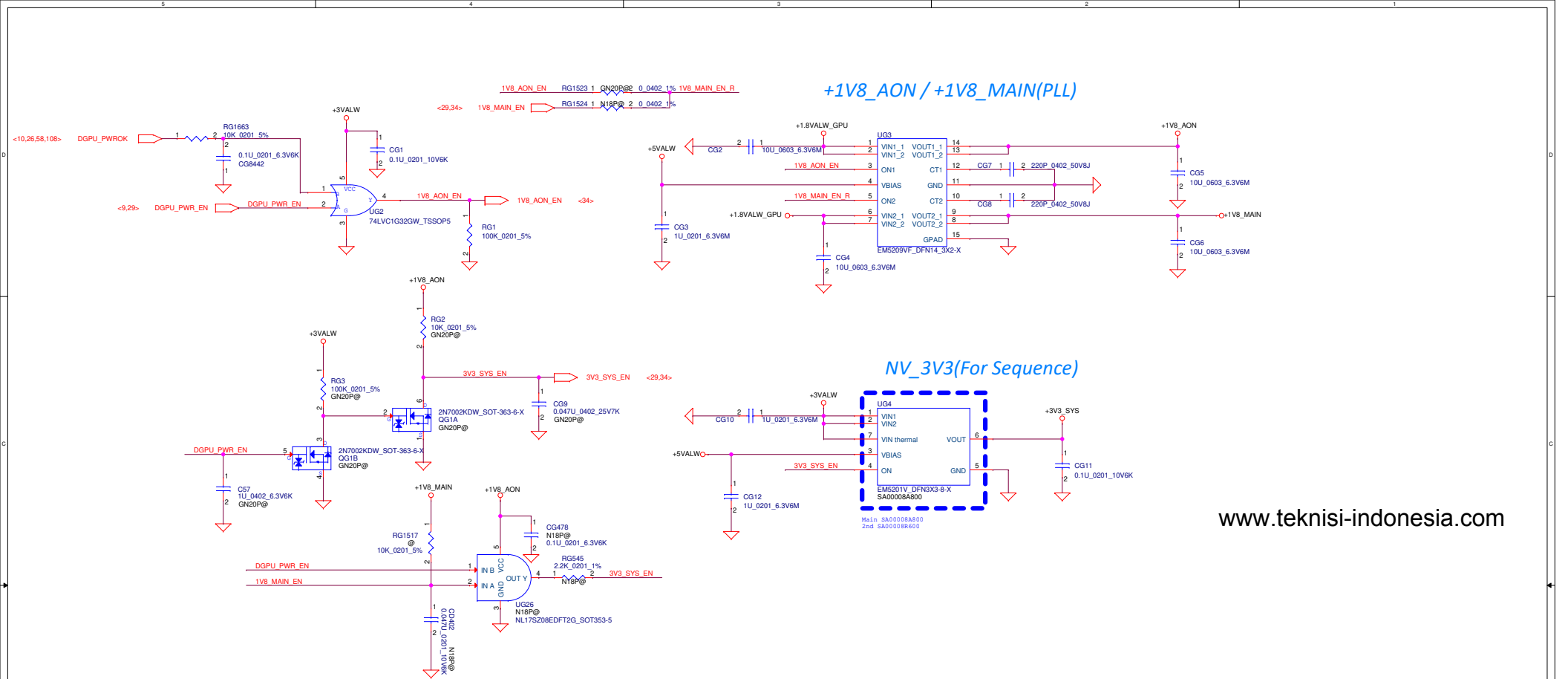
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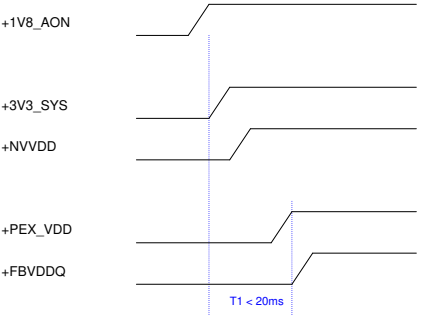
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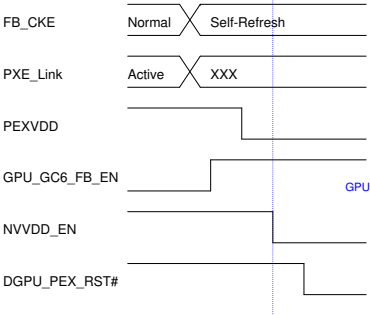
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GPU Power Up Sequence



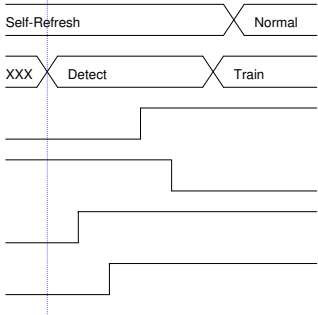
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

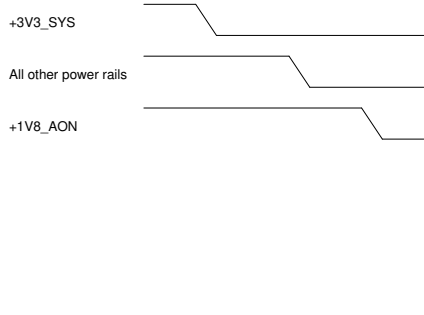


The entire entry/exit sequence must complete within 200 ms.

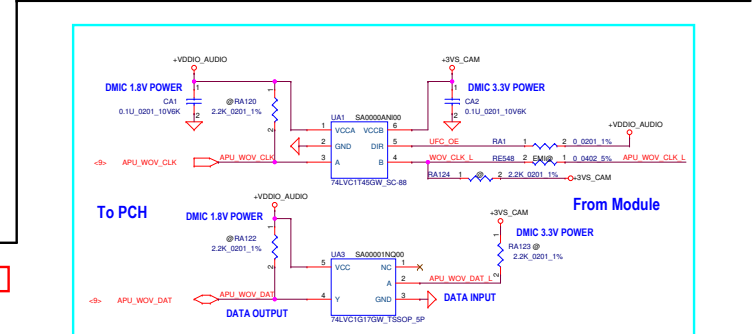
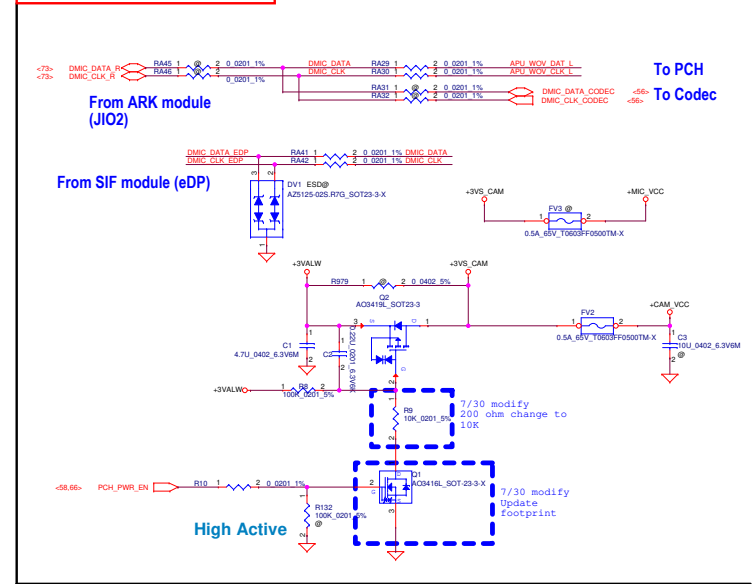
GPU GC6 Exit Sequence



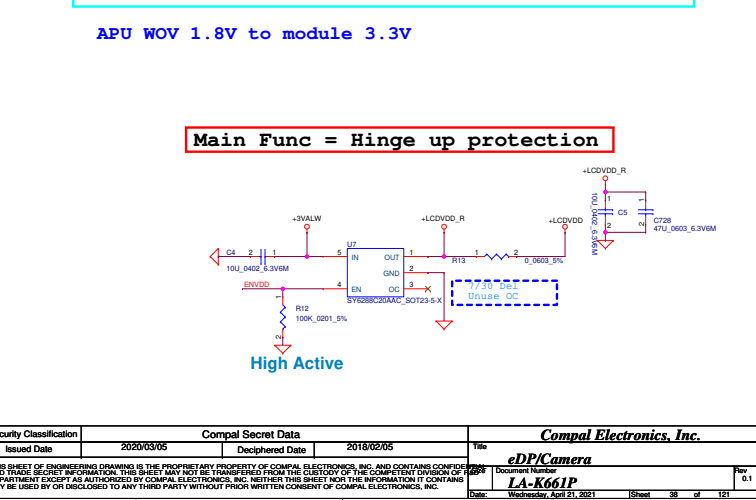
GPU Power Down Sequence



Main Func = DMIC



LCD EN **Main Func = Hinge up protection**



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Issued Date	2020/03/05	Deciphered Date	2018/02/05	File
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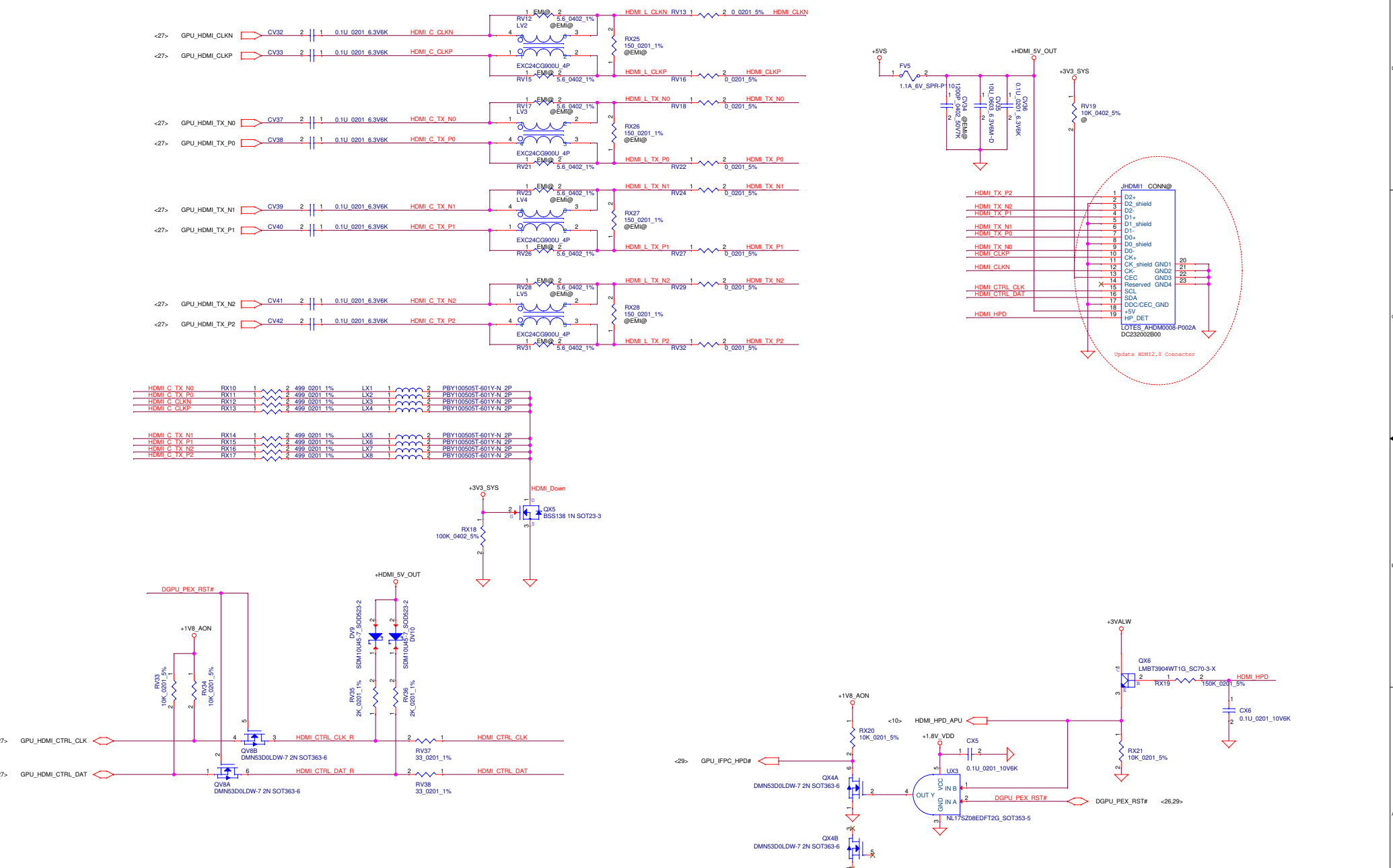
Main Func = DDS

Reserve

Main Func = eDP MUX

Reserve

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2020/03/05		2019/04/01		Document Number	
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				Date	
				Wednesday, April 21, 2021	
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Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HDMI	
2020/03/05		2018/02/05		Document Number	
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Main Function:

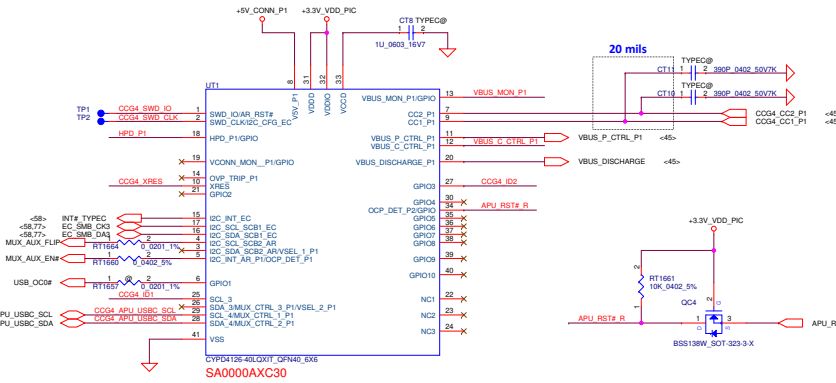
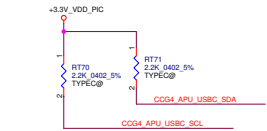
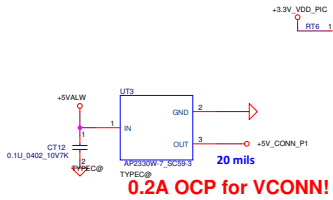
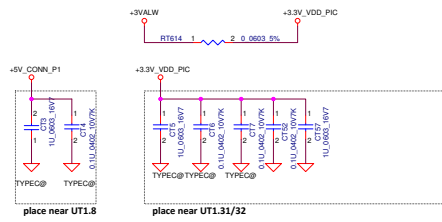
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				LA-K661P	0.1
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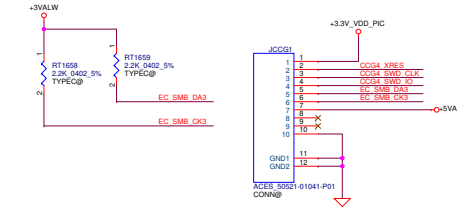
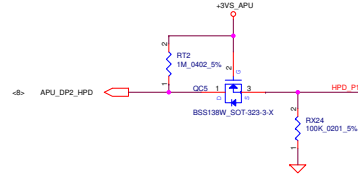


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Issued Date	2018/03/29	Deciphered Date	2019/03/29	Thunderbolt (1/2)	
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Issued Date	2018/03/29	Deciphered Date	2019/03/29	Title	Thunderbolt (2/2)
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				LA-K661P	
				Date: Wednesday, April 21, 2021	Sheet 43 of 121

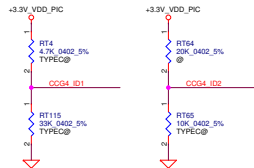


Type-C DP HPD



Parameter	Min(V)	Mux(V)	Current (A)
VDD1D	3V	5.5V	30mA
VDDIO	1.71V	5.5V	
V5V_P1	4.85V	5.5V	500mA
V5V_P2	4.85V	5.5V	500mA
CC1	3.3V	5V	10mil
CC2	3.3V	5V	10mil

MODID
CCG4 ID1: L7
CCG4 ID2: L0

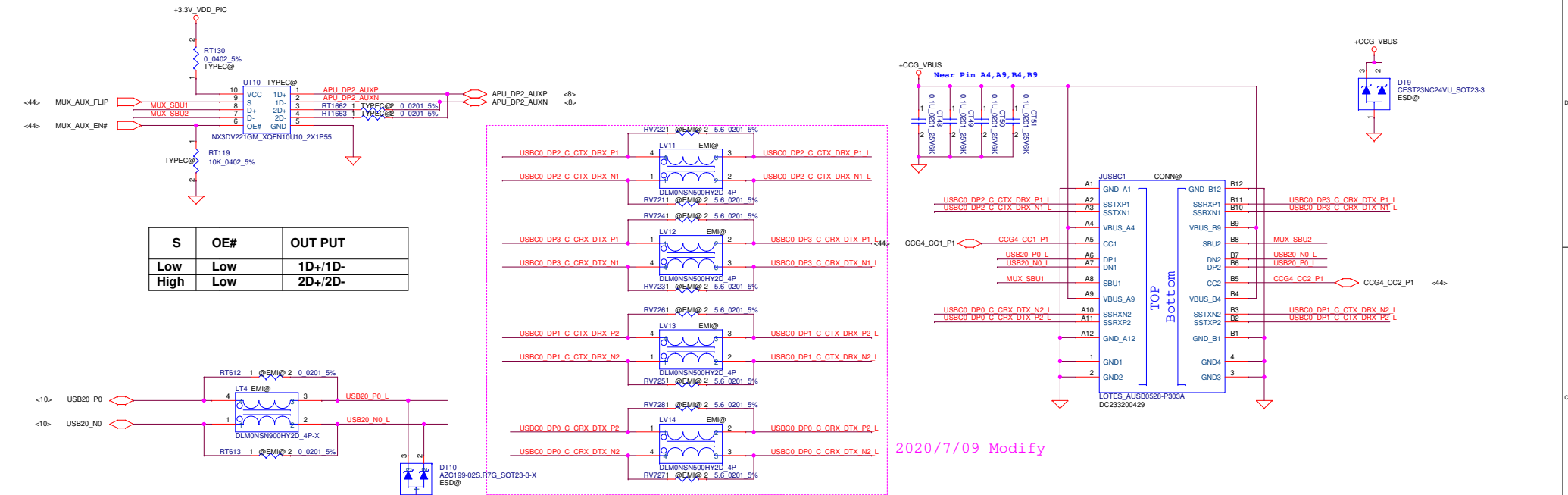


Voltagres for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Amanti 13" & 14"	L7	L7
2	Single Port - Intel - DDM support - Kyboren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL-R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

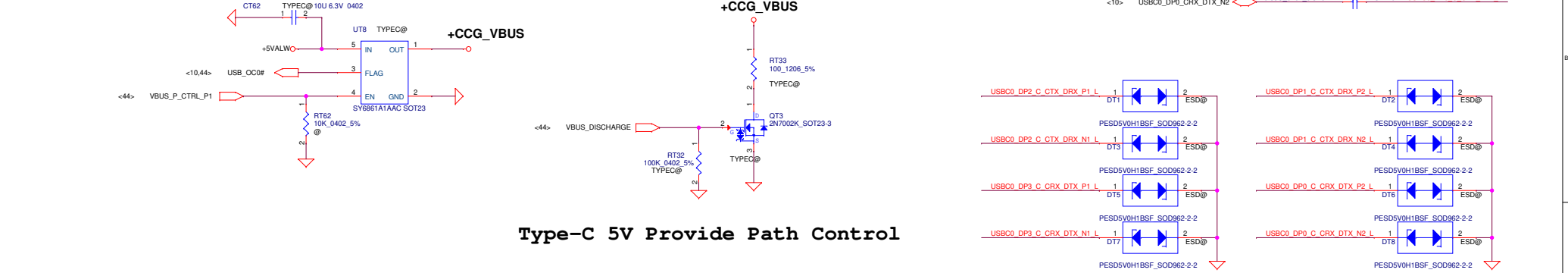
Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8

Main Function:



2020/7/09 Modify

5V@3A



Type-C 5V Provide Path Control

Main Function:

www.teknisi-indonesia.com

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				Date:	Wednesday, April 21, 2021	Sheet 48 of 121

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Main Function:

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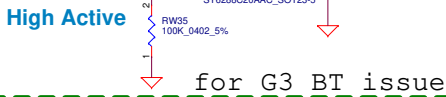
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				LA-K661P	0.1
				Date: Wednesday, April 21, 2021	Sheet 50 of 121

Main Function:

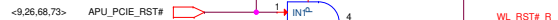
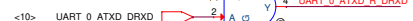
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Main Func = WLAN M.2



74	FSM	GPIO	76
72	FSM	RECEIVED_PACKETS	78
70	UM_Power_Sink/PowerSource	RECEIVED_PACKETS	79
68	UM_Power_Sink/PowerSource	RECEIVED_PACKETS	77
66	UM_Power_Sink/PowerSource	RECEIVED_PACKETS	67
64	RECEIVED	GPIO	65
62	ADAPTER	RECEIVED_PACKETS	63
60	RECEIVED_PACKETS	RECEIVED_PACKETS	61
58	RECEIVED_PACKETS	RECEIVED_PACKETS	59
56	RECEIVED_PACKETS	GPIO	57
54	RECEIVED_PACKETS	RECEIVED_PACKETS	55
52	RECEIVED_PACKETS	RECEIVED_PACKETS	53
50	SUSPEND	GPIO	51
48	RECEIVED_PACKETS	RECEIVED_PACKETS	49
46	RECEIVED_PACKETS	RECEIVED_PACKETS	47
44	RECEIVED_PACKETS	RECEIVED_PACKETS	45
42	VENDOR_DEFINED	RECEIVED_PACKETS	43
40	VENDOR_DEFINED	RECEIVED_PACKETS	41
38	VENDOR_DEFINED	RECEIVED_PACKETS	39
36	UART_1TX	RECEIVED_PACKETS	37
34	UART_1TX	GPIO	35
32	UART_1TX	GPIO	33
21	UART_1TX	GPIO	23
20	UART_1TX	GPIO	21
18	GPIO	GPIO	19
16	GPIO	GPIO	17
14	GPIO	GPIO	15
12	GPIO	GPIO	13
10	GPIO	GPIO	11
8	GPIO	GPIO	9
6	GPIO	GPIO	7
4	GPIO	GPIO	5
2	GPIO	GPIO	3



Main Function:

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				Date:	Wednesday, April 21, 2021	Sheet 53 of 121

Main Function:

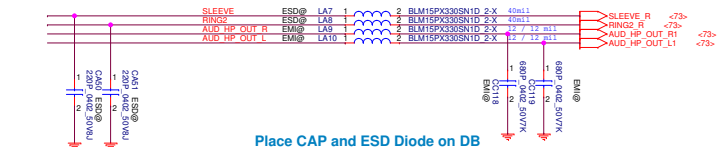
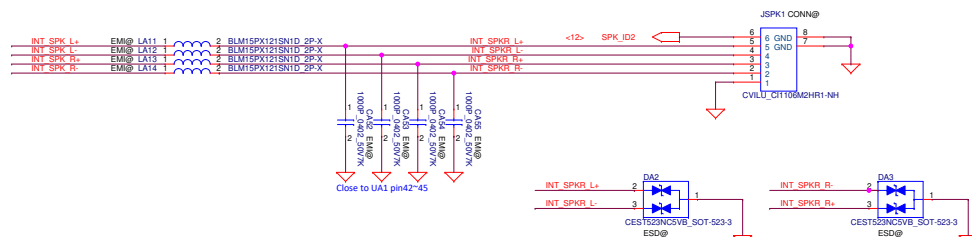
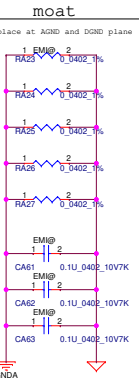
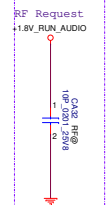
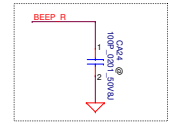
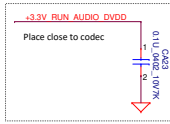
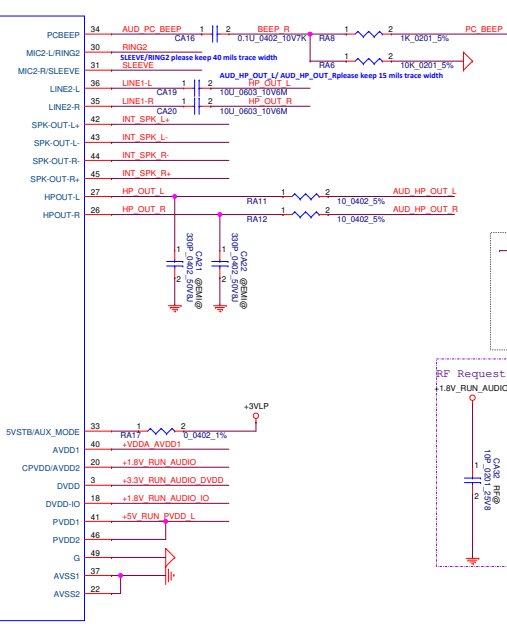
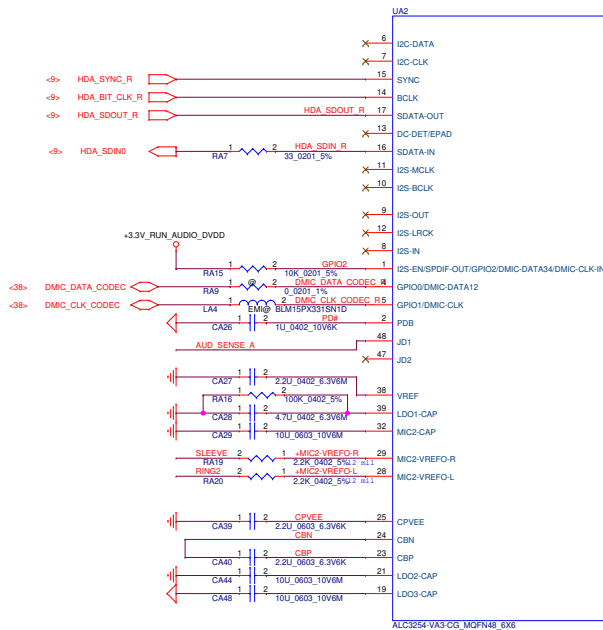
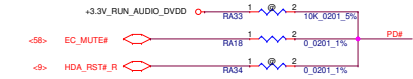
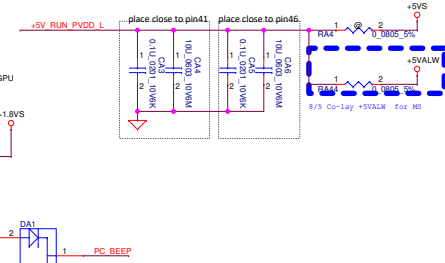
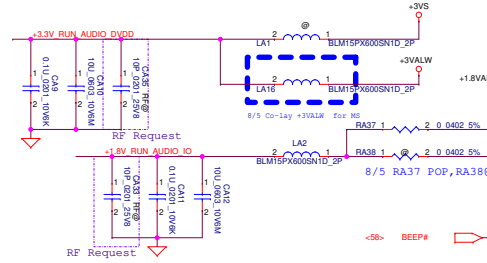
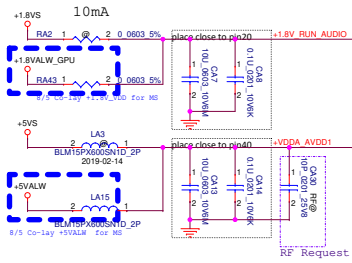
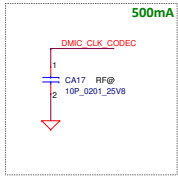
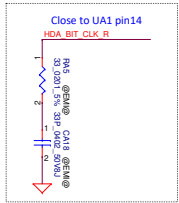
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				LA-K661P	0.1
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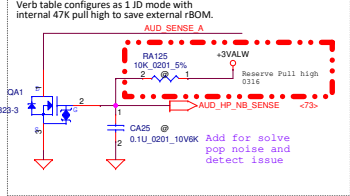
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Place CAP and ESD Diode on DB

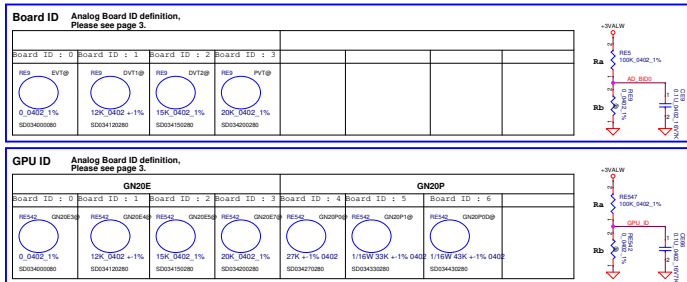


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Date: Wednesday, April 21, 2021		Sheet 56 of 121	

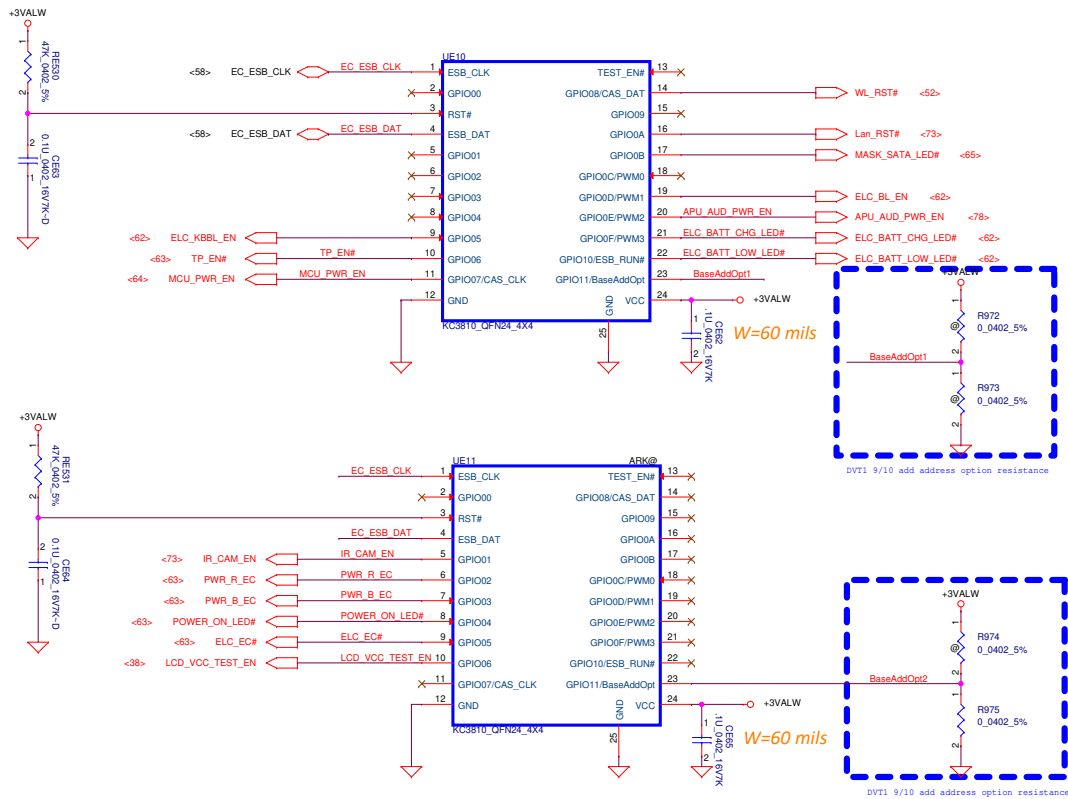
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				LA-K661P	0.1
				Date: Wednesday, April 21, 2021	Sheet 57 of 121

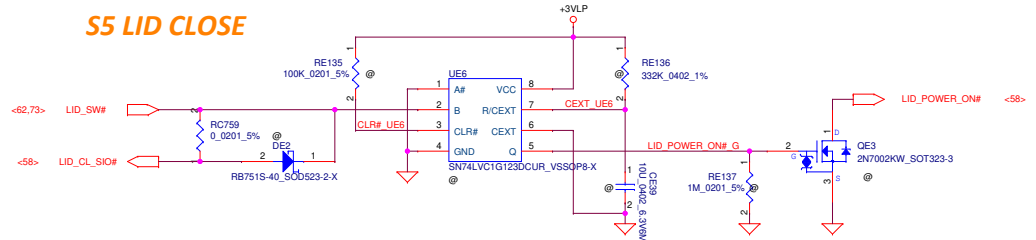


Main Func = GPIO Expander



FUNCTION TABLE

INPUTS			OUTPUTS
CLR	\bar{A}	B	Q
L	X	X	L
X	H	X	L (1)
X	X	L	L (1)
H	L	\uparrow	\square
H	\downarrow	H	\square
\uparrow	L	H	\square



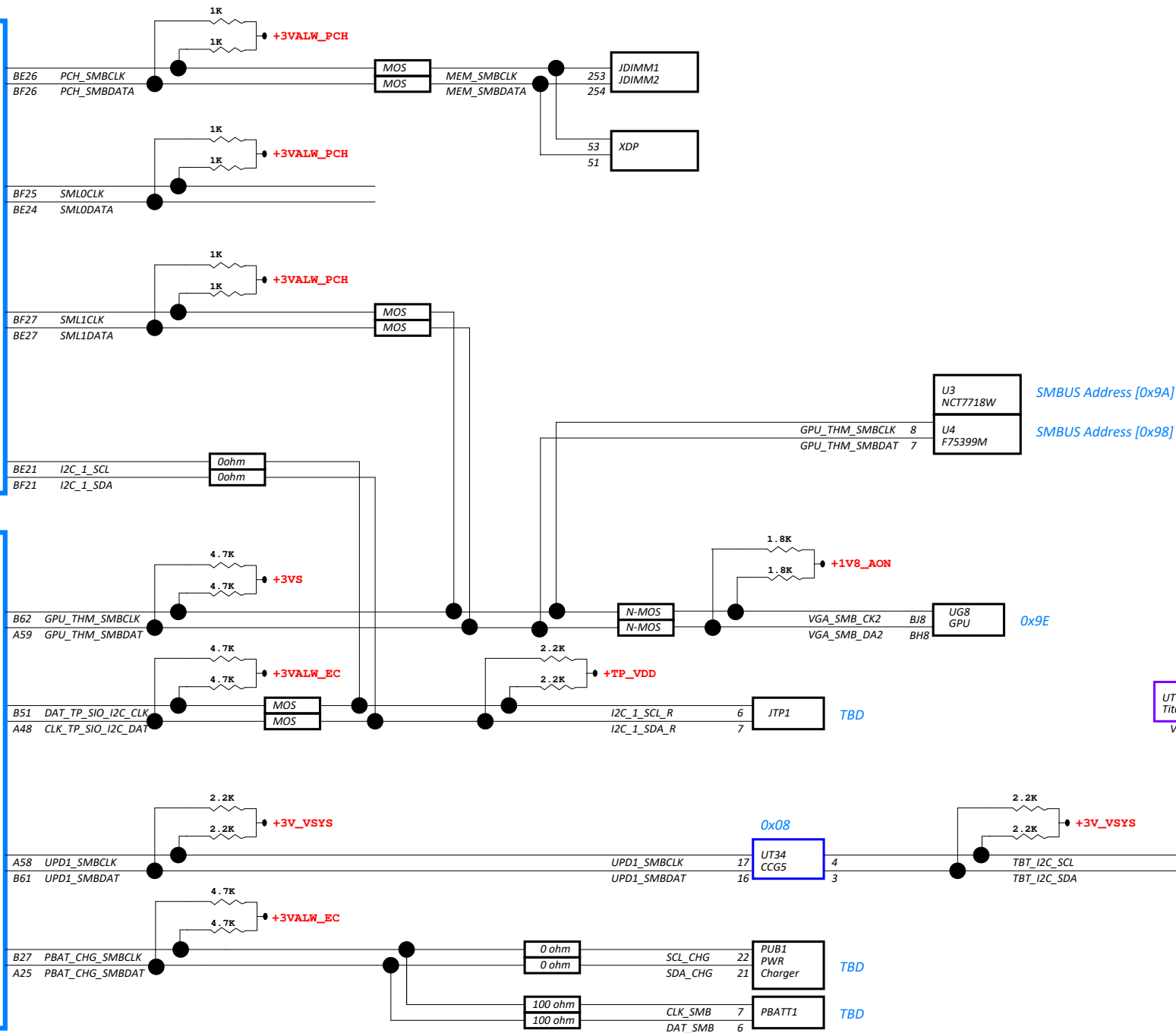
Main Function:

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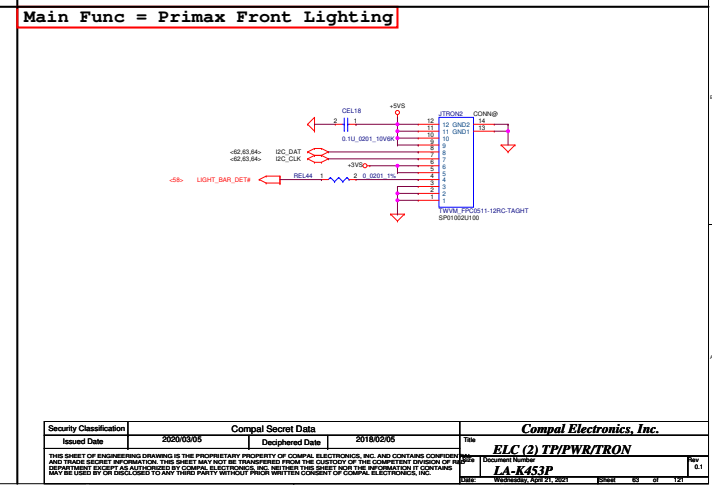
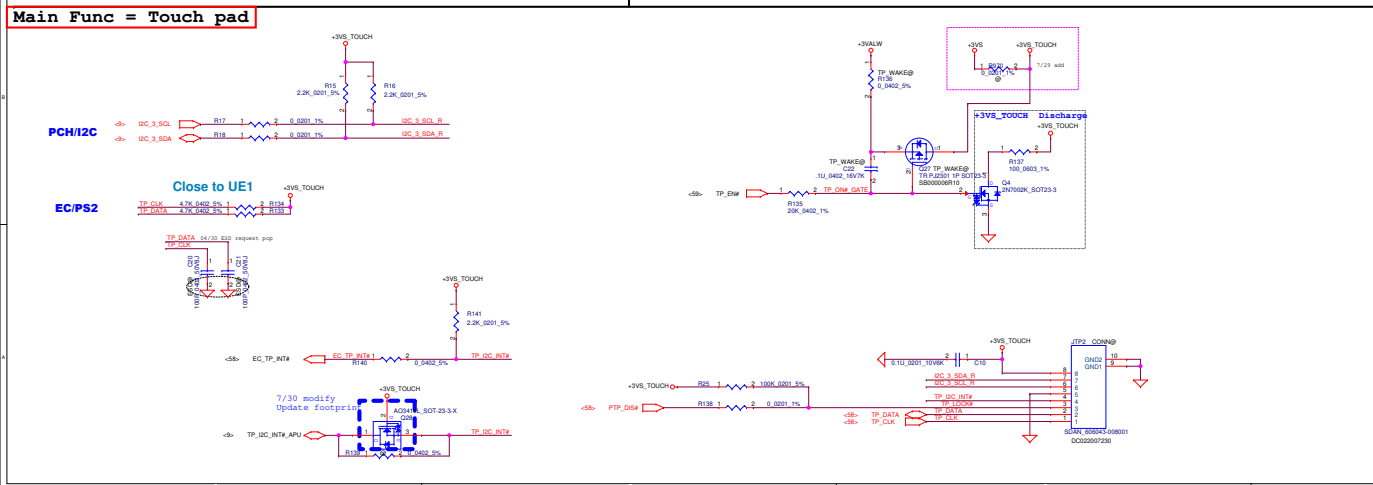
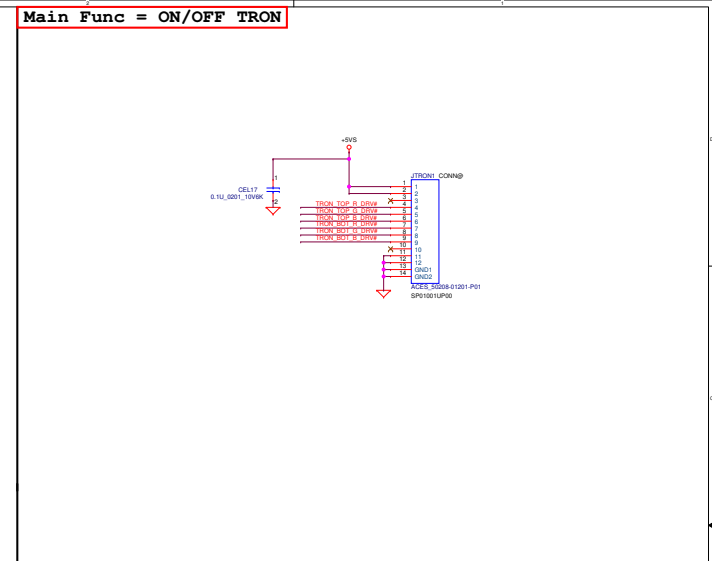
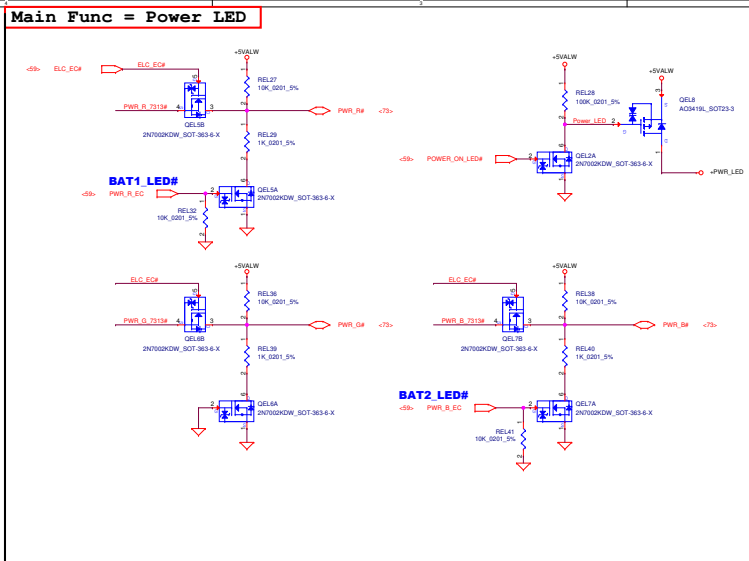
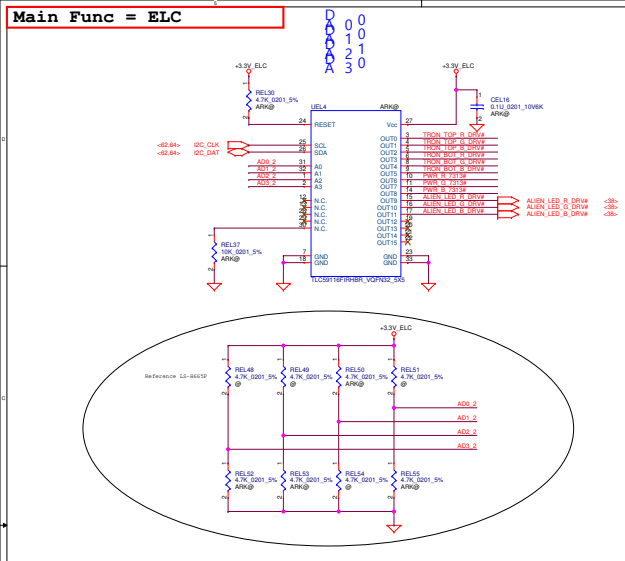
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MEMC15

MEMC15



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				LA-K661P			
				Date	Wednesday, April 21, 2021		Sheet

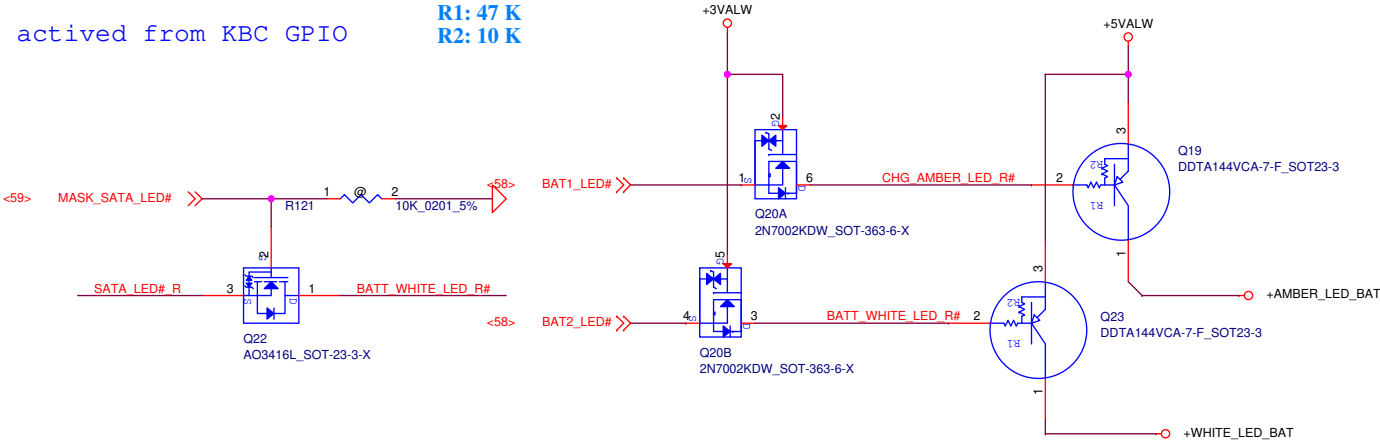


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				ELC (2) TP/PWR/TRON
				LA-K43P
				Rev 6.1

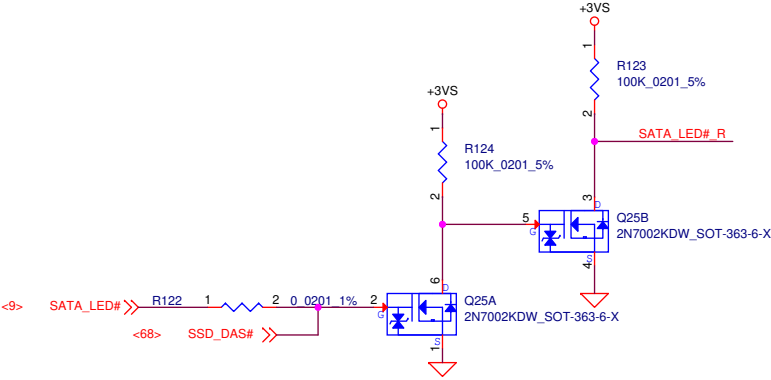
Main Func = Battery LED

Low actived from KBC GPIO

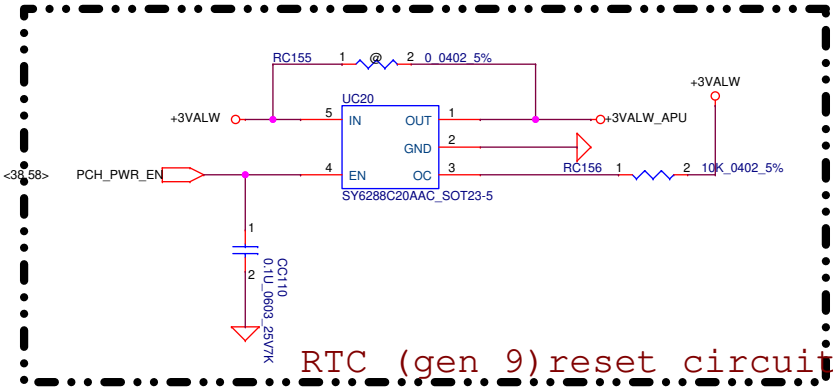
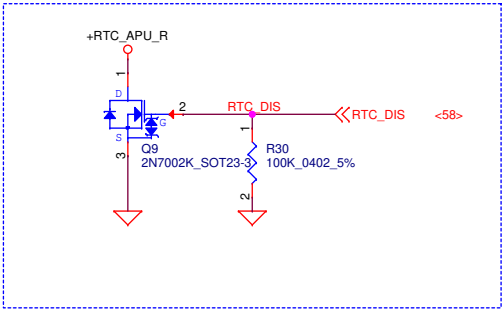
BJT
R1: 47 K
R2: 10 K



Main Func = M_BIST



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2019/04/01	Title	LED (SIF)
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				Date:	Wednesday, April 21, 2021
				Sheet	65 of 121
				Rev	0.1



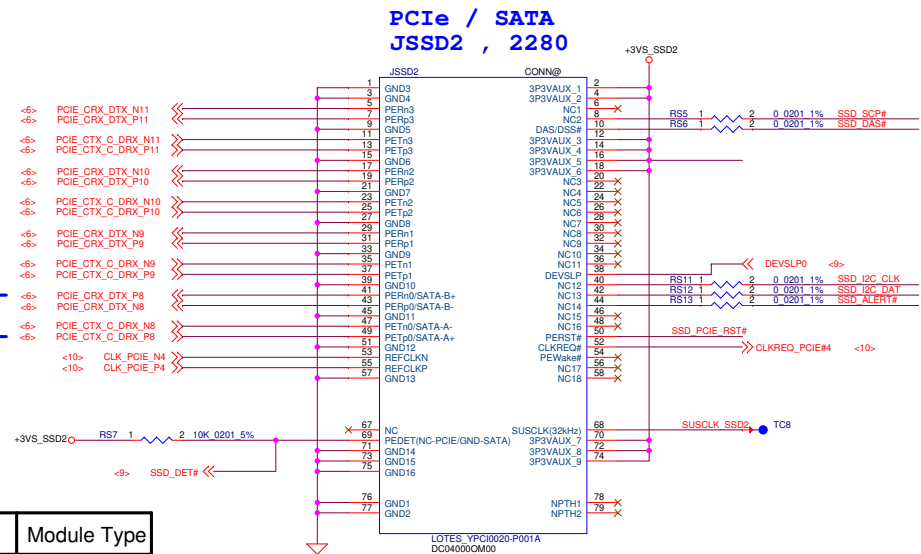
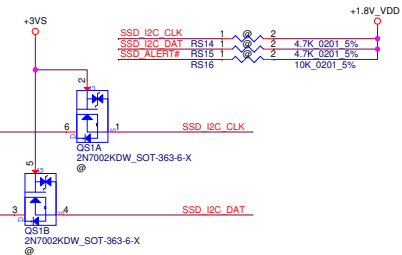
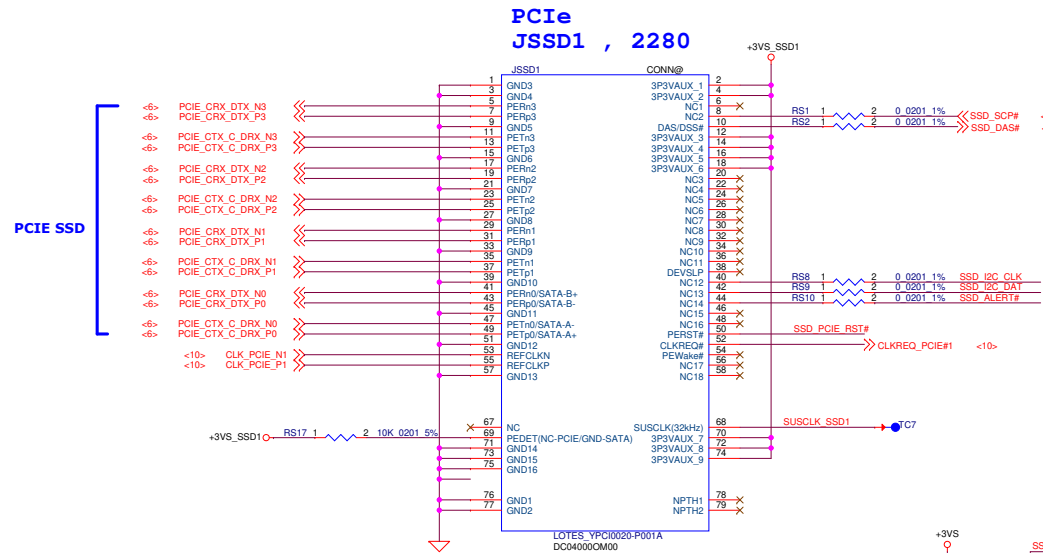
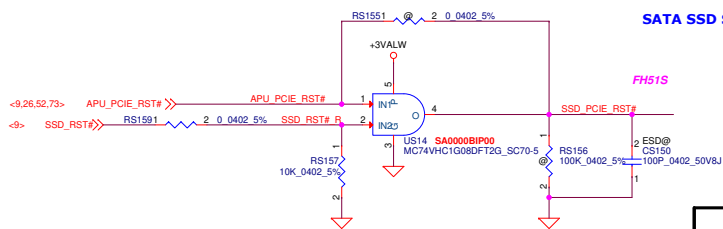
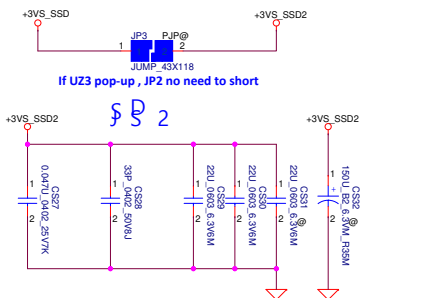
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2019/04/01	Title	
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				LA-K661P	0.1
Date: Wednesday, April 21, 2021				Sheet	66 of 121

Main Function:

Reserve

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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV
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				LA-K661P	0.1
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PEDET	Module Type
0	SATA
1	PCIe

Main Function:

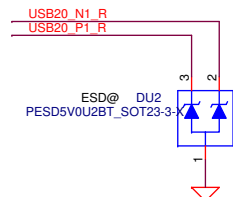
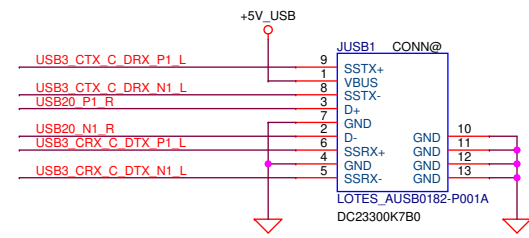
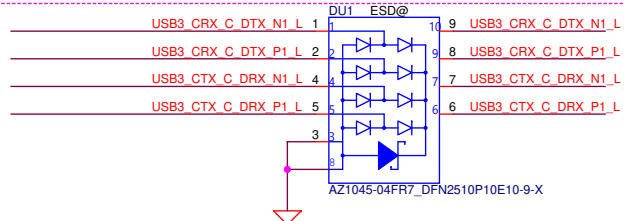
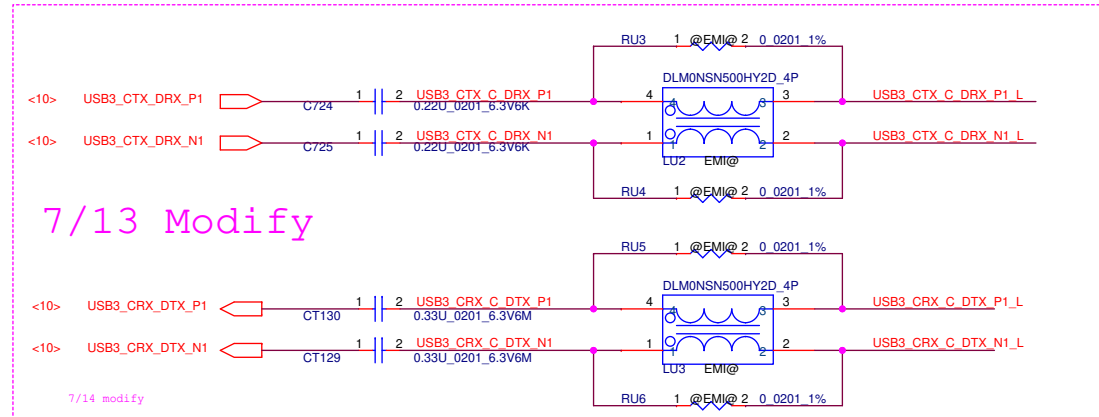
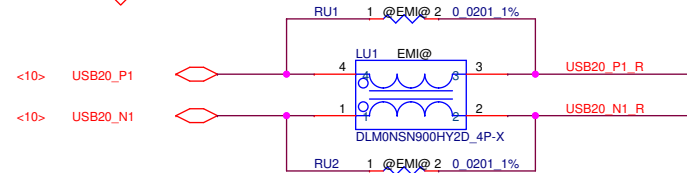
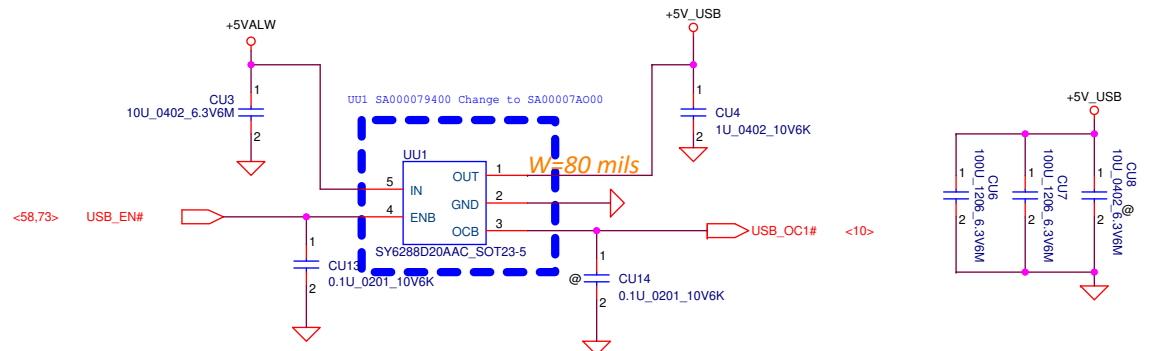
Reserve

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				LA-K661P	0.1
				Date: Wednesday, April 21, 2021	Sheet 69 of 121

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				Date:	Wednesday, April 21, 2021	Sheet 70 of 121

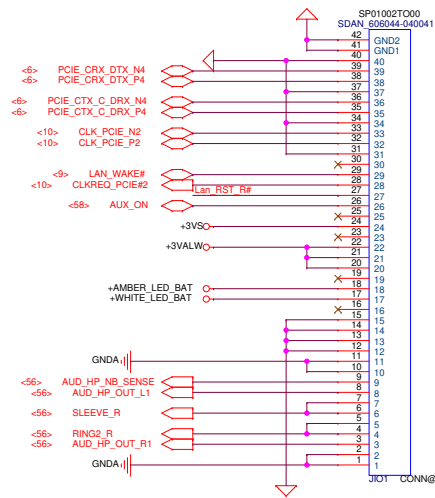
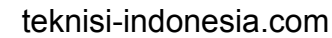


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	USB3.1 TypeA Gen1
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				Date:	Wednesday, April 21, 2021
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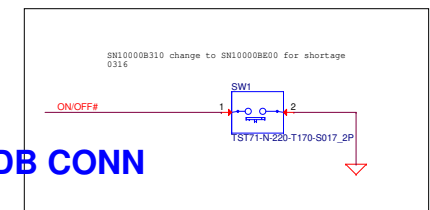
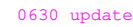
Main Function:

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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV
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For LAN DB CONN

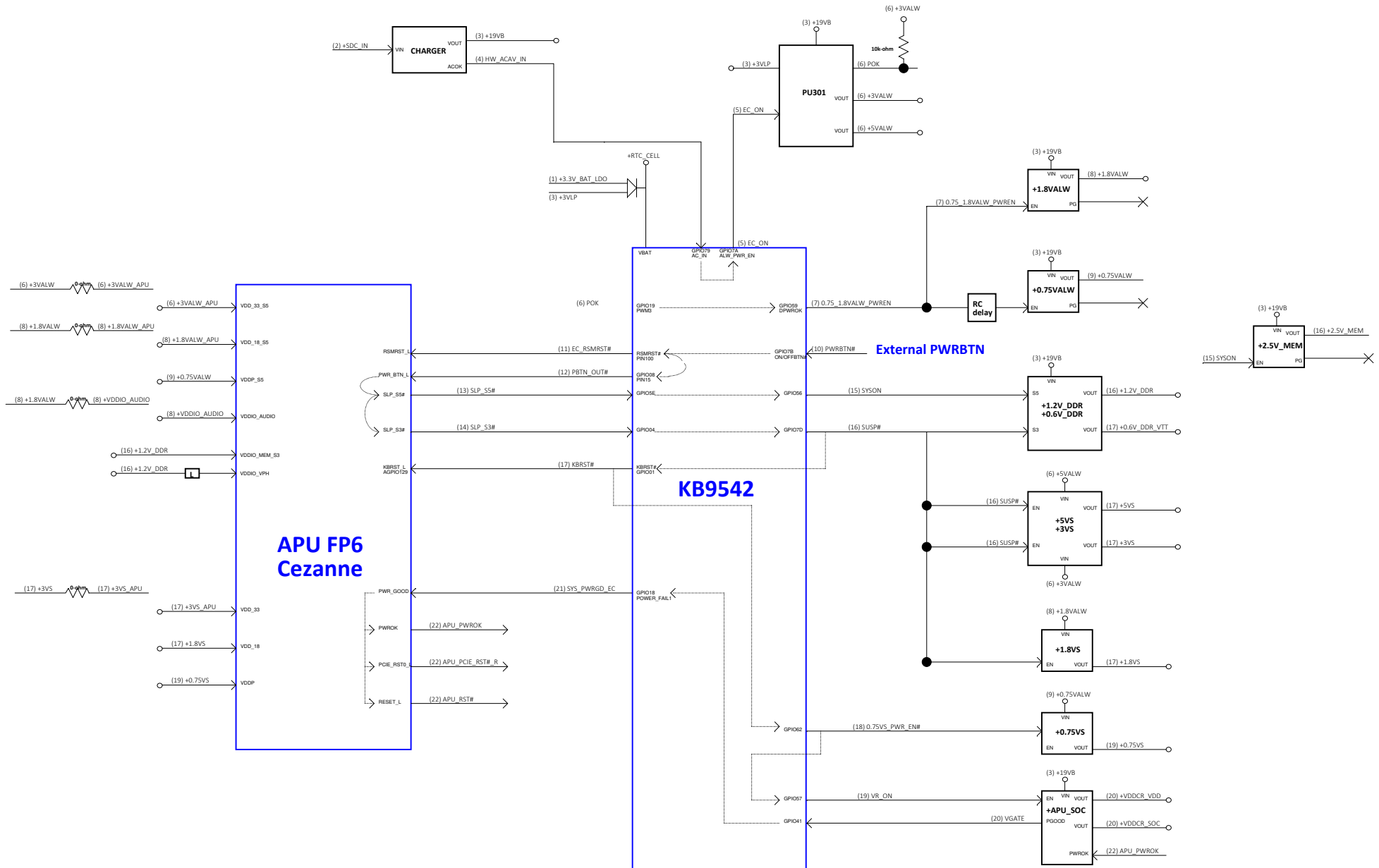


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2020/03/05	Deciphered Date	2018/02/05	Title	IO Board CONN	
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				LA-K661P		
Date:				Wednesday, April 21, 2021	Sheet	73 of 121

Main Function:

Reserve

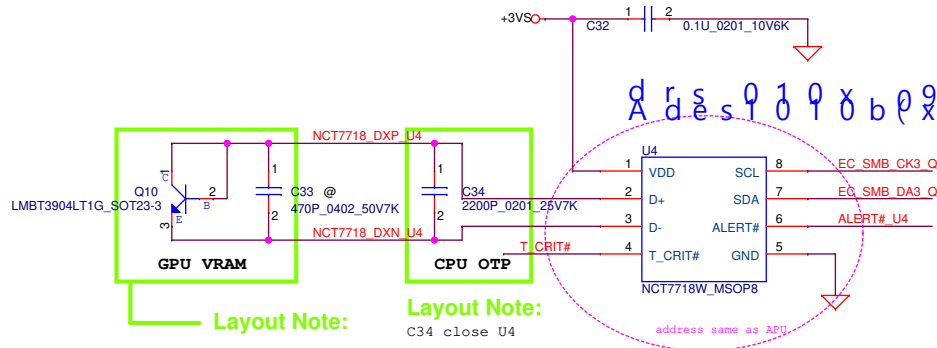
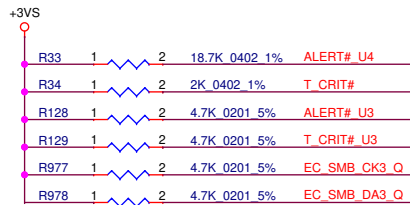
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2019/04/01	Title	DOCK(RSVD)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
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				Date: Wednesday, April 21, 2021	Sheet 74 of 121



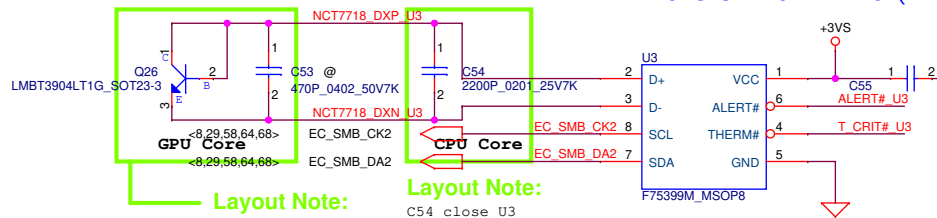
Main Function:

Reserve

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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	RSV	
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				Date:	Wednesday, April 21, 2021	Sheet 76 of 121



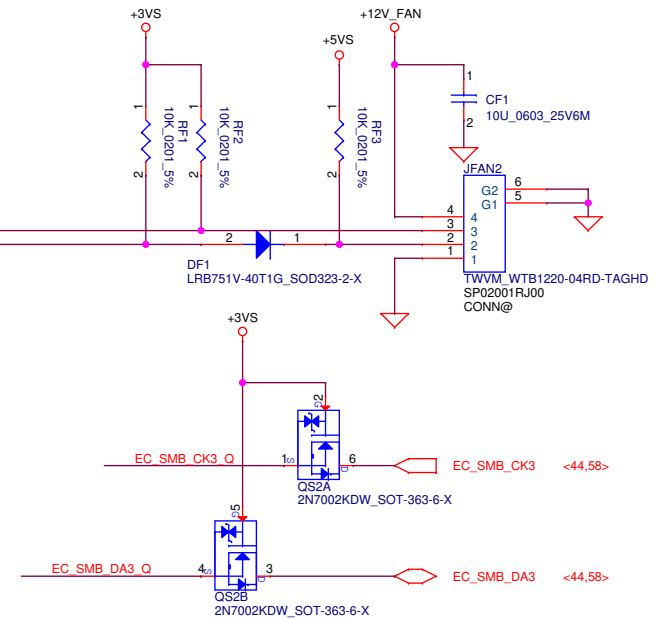
DXN and DXP routing width and spacing is 10 mil / 10 mil.



DXN and DXP routing width and spacing is 10 mil / 10 mil.

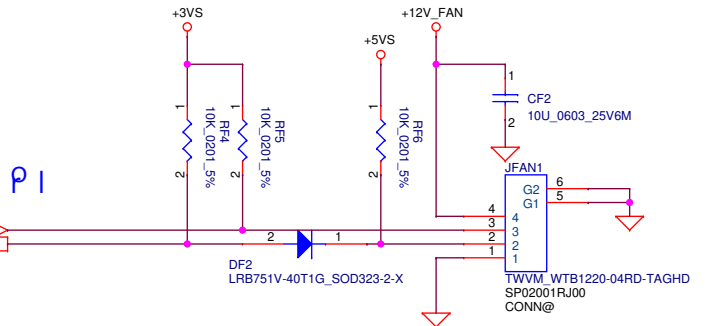
EC SMB CK3 Q
EC SMB DA3 Q
ALERT# U4
T CRIT# U4

PWM_FAN1
TACH_FAN1



EC SMB CK3 Q
EC SMB DA3 Q
ALERT# U3
T CRIT# U3

PWM_FAN2
TACH_FAN2

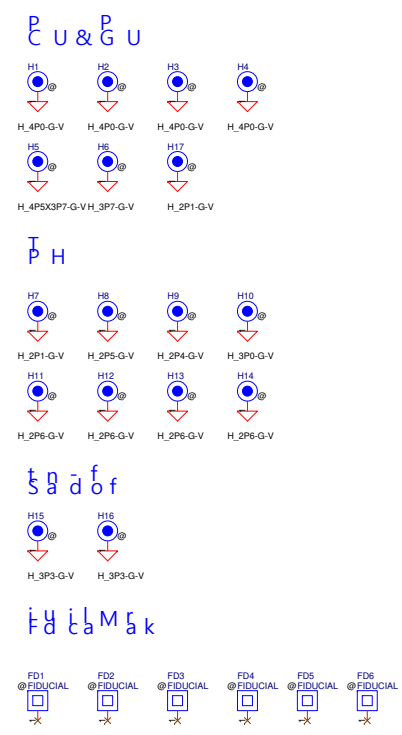
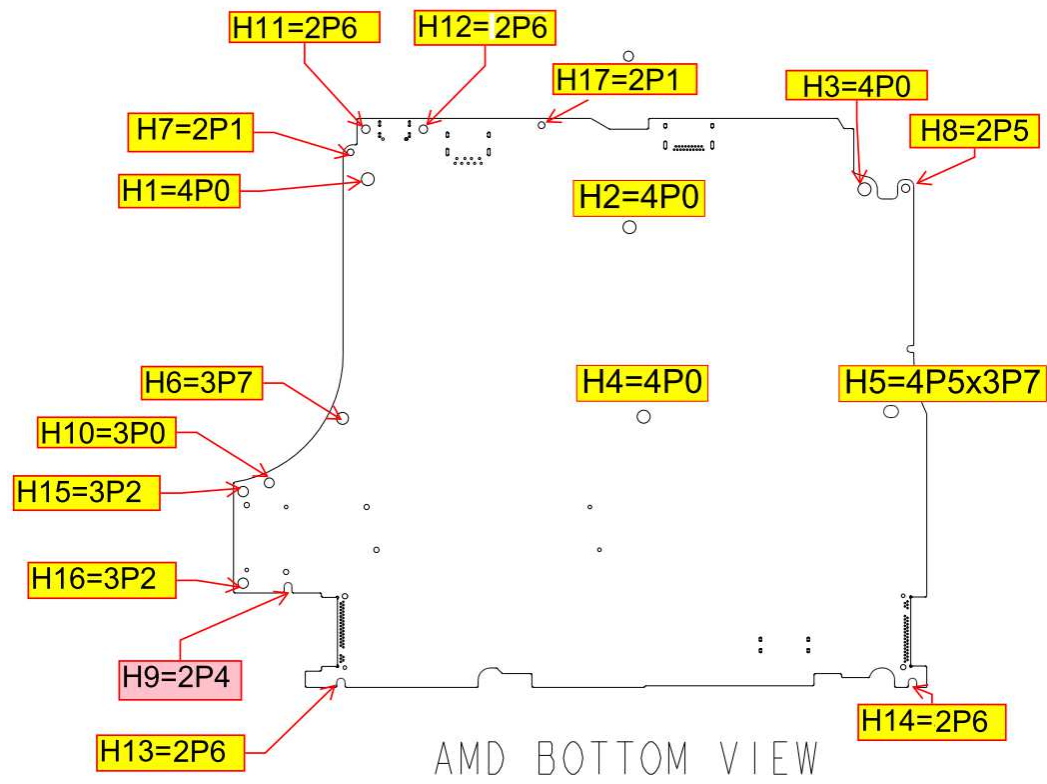


TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2018/02/05	Title	FAN/Thermal
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BIOS UART Debug

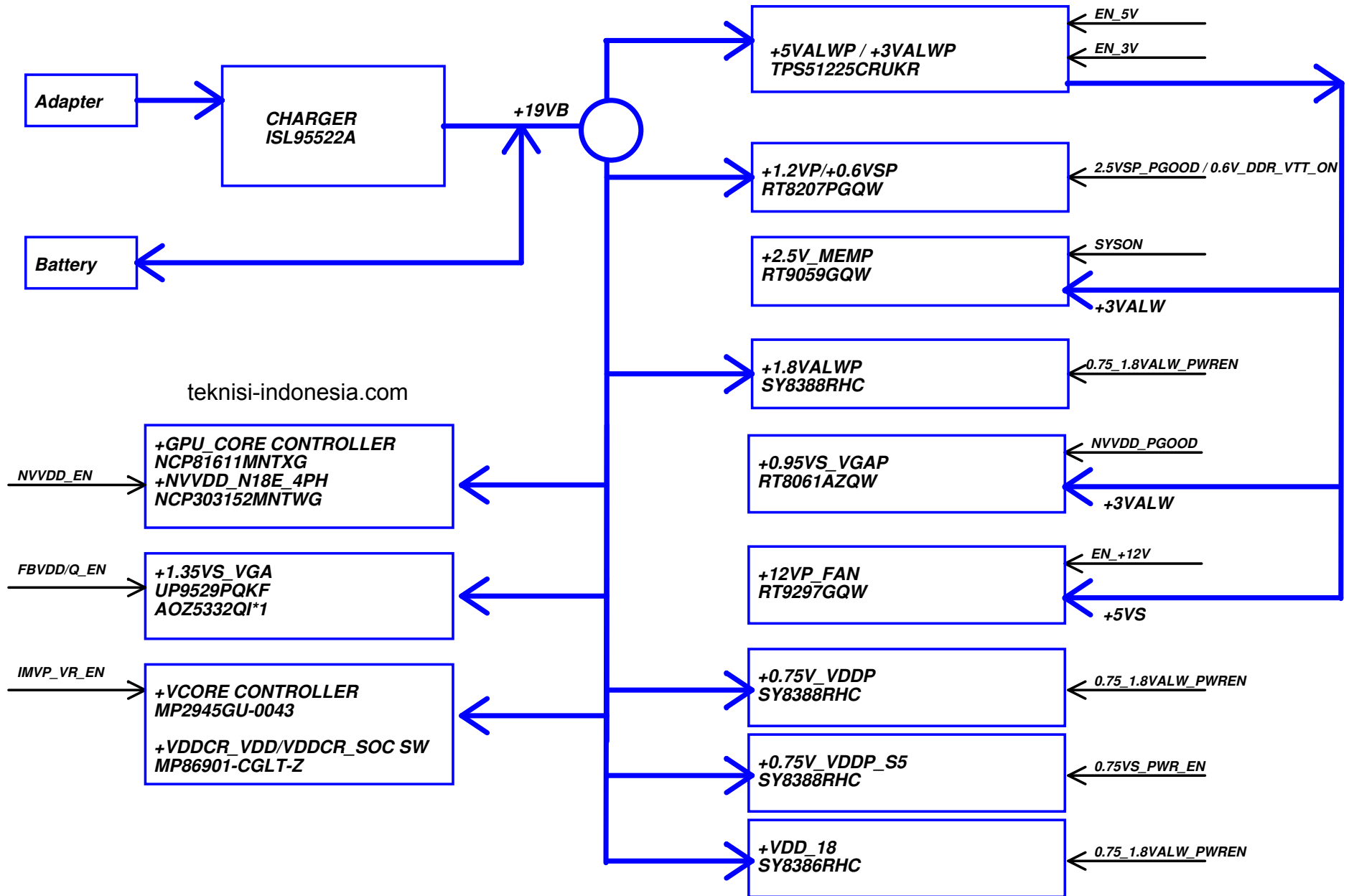
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2018/10/01	Title	Debug APS,DEG
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
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AMD BOTTOM VIEW

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2018/02/05	Title	Screw Hole
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				Date	Wednesday, April 21, 2021
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				Rev	0.1

Power block



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2021/08/01	Title	PWR POWER BLOCK DIAGRAM
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Main Func = DCIN CONN

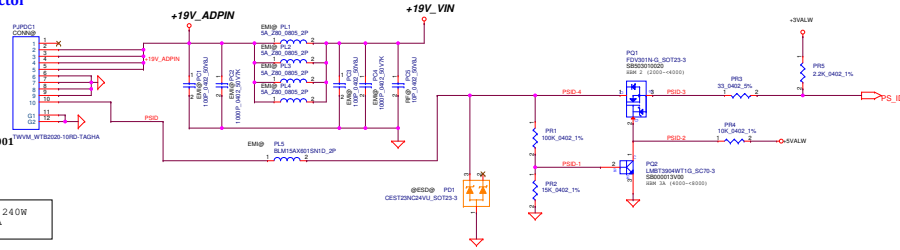
Adapter Connector

Adapter Bot Side

PIN1 N/A
PIN2 ADFIN
PIN3 ADFIN
PIN4 ADFIN
PIN5 ADFIN
PIN6 GND
PIN7 GND
PIN8 GND
PIN9 GND
PIN10 PSID
ACES_50459-010H0M0-001

CONN1
 1
 2
 3
 4
 5
 6
 7
 8
 9
 10
 G1
 G2

T2WM_WTB2002-10FD-T2H2R



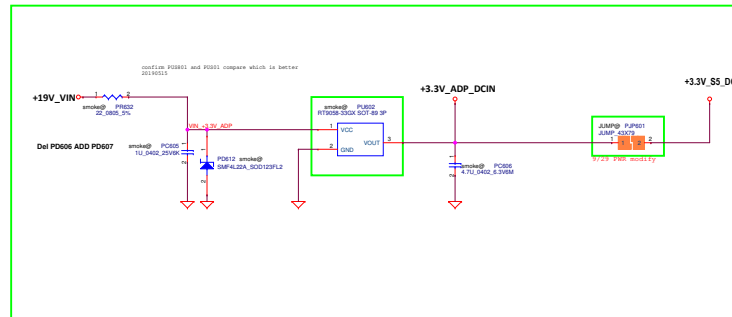
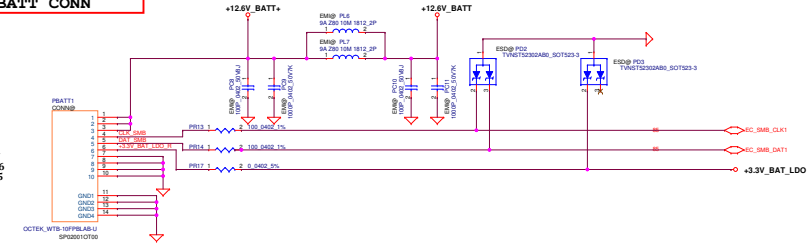
Adapter 180W / 240W
240W/19V=12.63A

Main Func = BATT CONN

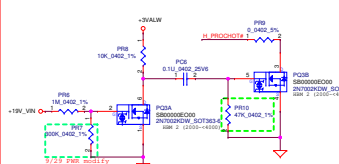
Battery Connector

Battery Bot Side
Before ->After
PIN1 GND->PIN 10
PIN2 GND->PIN0 9
PIN3 GND->PIN0 8
PIN4 SYS_PRES#->PIN0 7
PIN5 BATT_PR#->PIN0 6
PIN6 DAT_SMB#->PIN0 5
PIN7 CLK_SMB#->PIN0 4
PIN8 BATT+>PIN0 3
PIN9 BATT+>PIN0 2
PIN10 BATT+>PIN0 1
SP07001R500

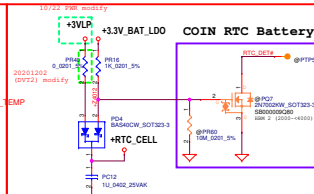
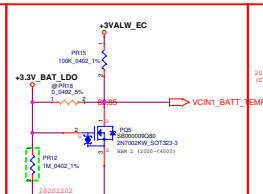
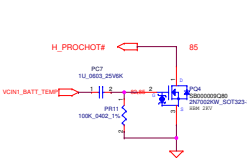
Battery 56W
56W/11.4V-4.91A
Battery 86W
86W/11.4V-7.54A



Adapter protection:

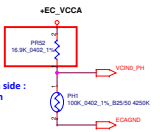



Battery protection:



APU OTP

PH1 under CPU bottom side :
CPU thermal protection
at 92 +/- 3 degree C



Security Classification	Compel Secret Data			
Issued Date	2016/03/05	Deciphered Date	2017/01/06	
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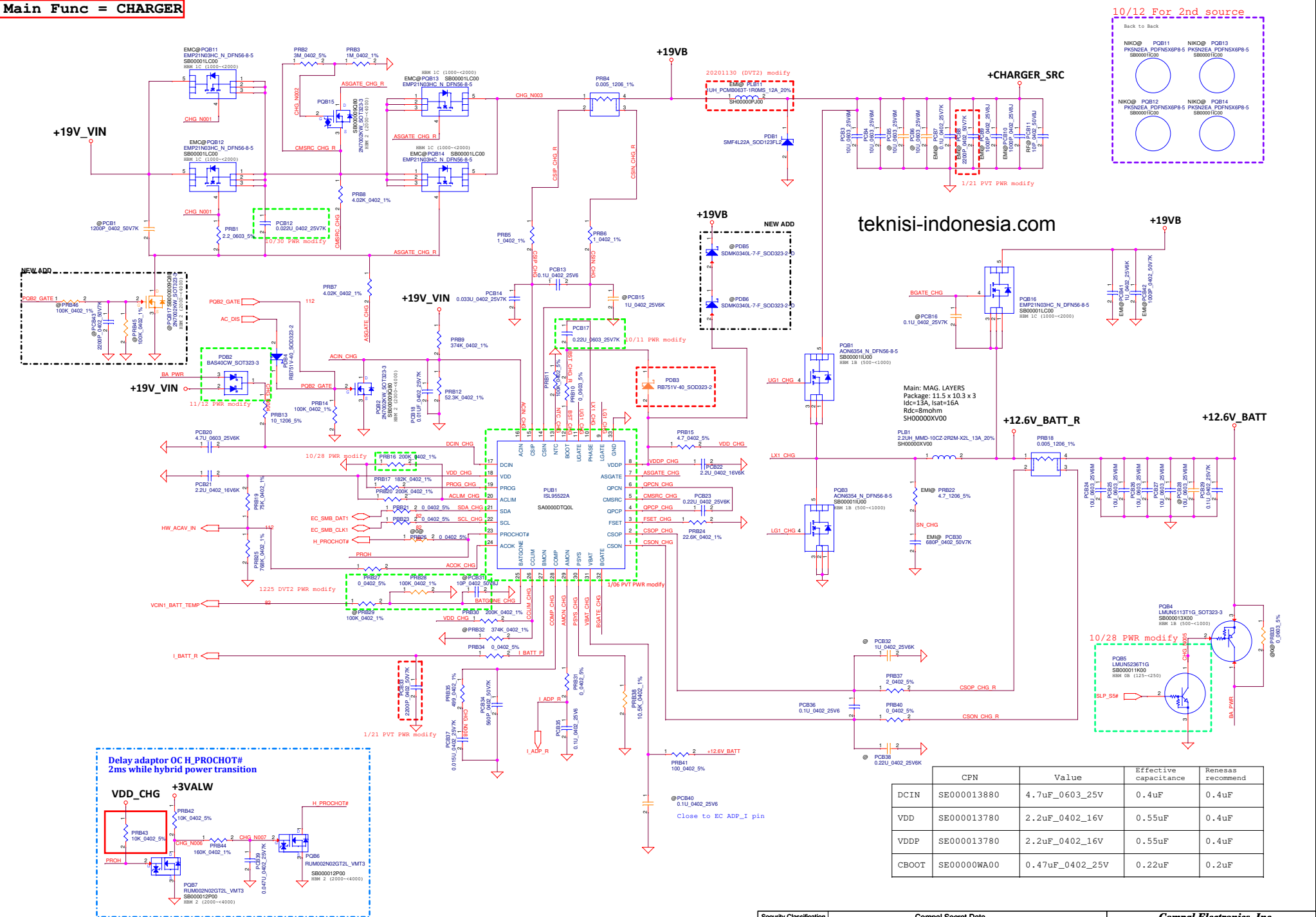
Reserve for PWR

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR	
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Reserve for PWR

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR	
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Main Func = CHARGER



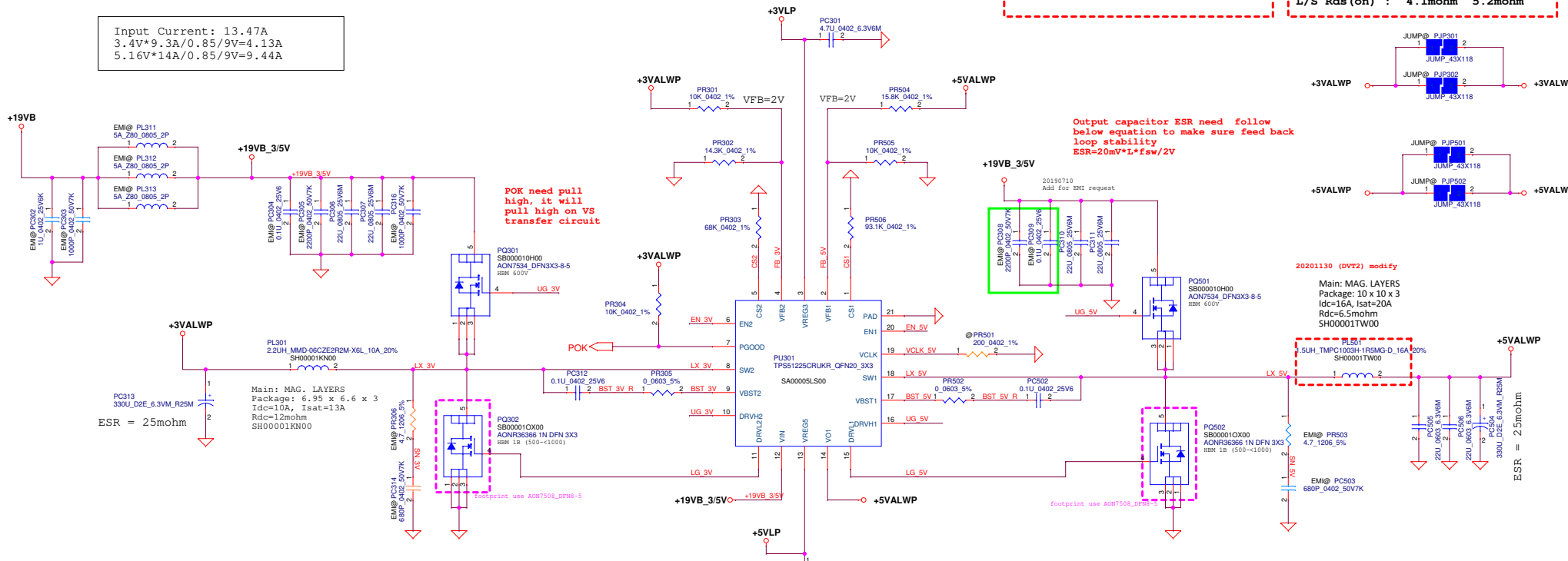
	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

Reserve for PWR

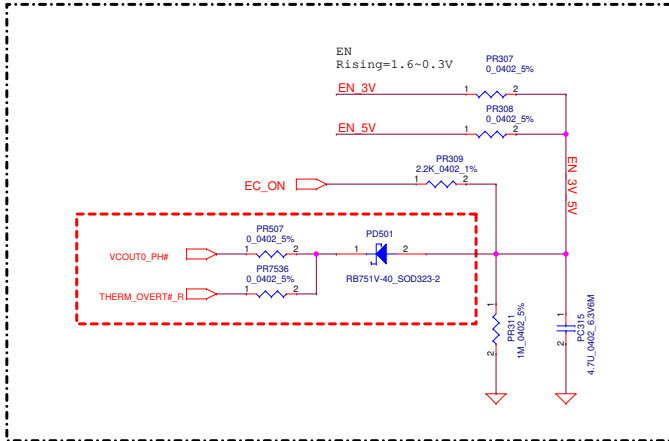
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR
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Main Func = 3VALWP / 5VALWP

Input Current: 13.47A
 $3.4V \times 9.3A / 0.85 / 9V = 4.13A$
 $5.16V \times 14A / 0.85 / 9V = 9.44A$



2020/07/06 HW control



Security Classification	Compal Secret Data			Title	
Issued Date	2020/03/05	Deciphered Date	2018/12/31	PWR +3.3VALWPA+5VALWPA LA-K454P	
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				Date: Wednesday, April 2, 2021	Sheet 87 of 125

Reserve for PWR

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				LA-K453P	0.1
Date: Wednesday, April 21, 2021				Sheet	88 of 121

Main Func = 1.2VP / 0.6VSP / 2.5V_MEMP

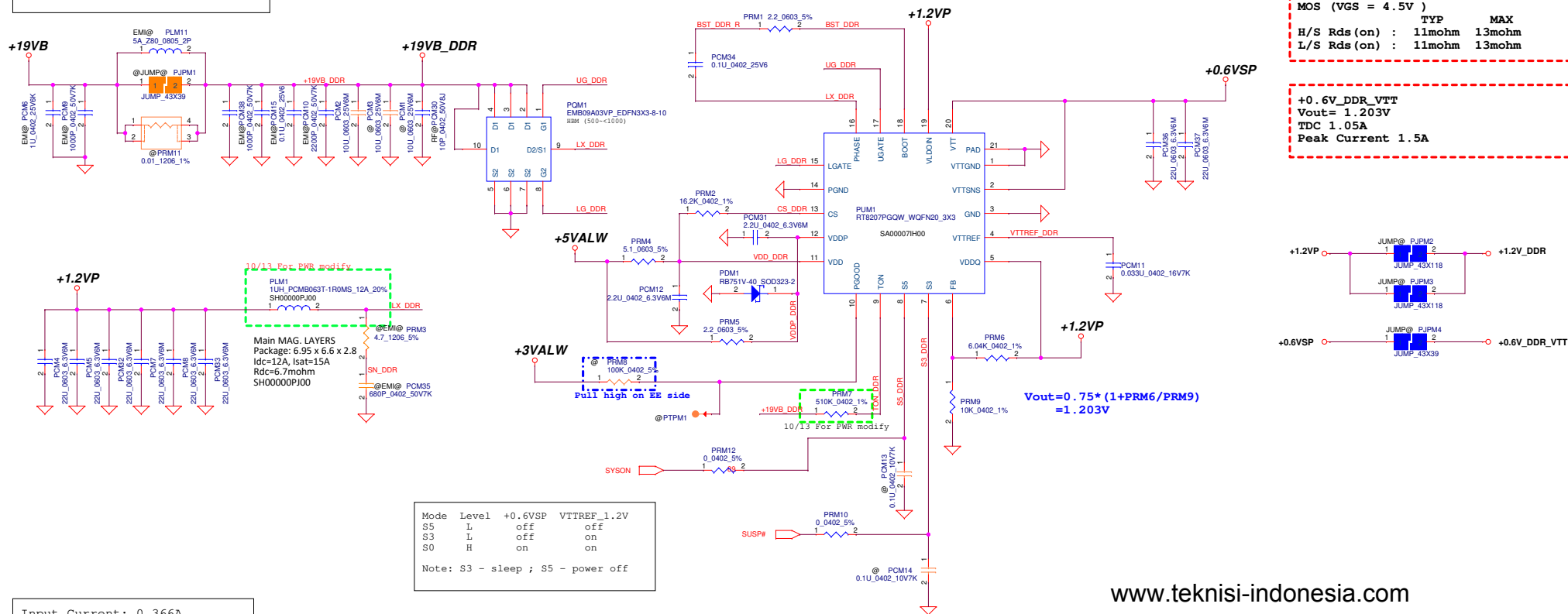
Input Current: 1.332A
 $1.203V \times 8A / 0.85 / 9V = 1.25A$
 $0.6V \times 1.05A / 0.85 / 9V = 0.082A$

Pin19 need pull separate from +1.2VP.
 If you have +1.2V and +0.6V sequence question,
 you can change from +1.2VP to +1.2VS.

+1.2V_DDR
 Vout= 1.203V
 TDC 6.6A
 Peak Current 9.4A
 OCP current 12.22A
 OVP=1.36V~1.44V (113%~120%)
 UVP=0.72V~0.96V (60%~80%)
 FSW= ~538KHz

MOS (VGS = 4.5V)
 TYP MAX
 H/S Rds (on) : 11mohm 13mohm
 L/S Rds (on) : 11mohm 13mohm

+0.6V_DDR_VTT
 Vout= 1.203V
 TDC 1.05A
 Peak Current 1.5A



Input Current: 0.366A
 $2.52V \times 0.37A / 0.85 / 3V = 0.366A$

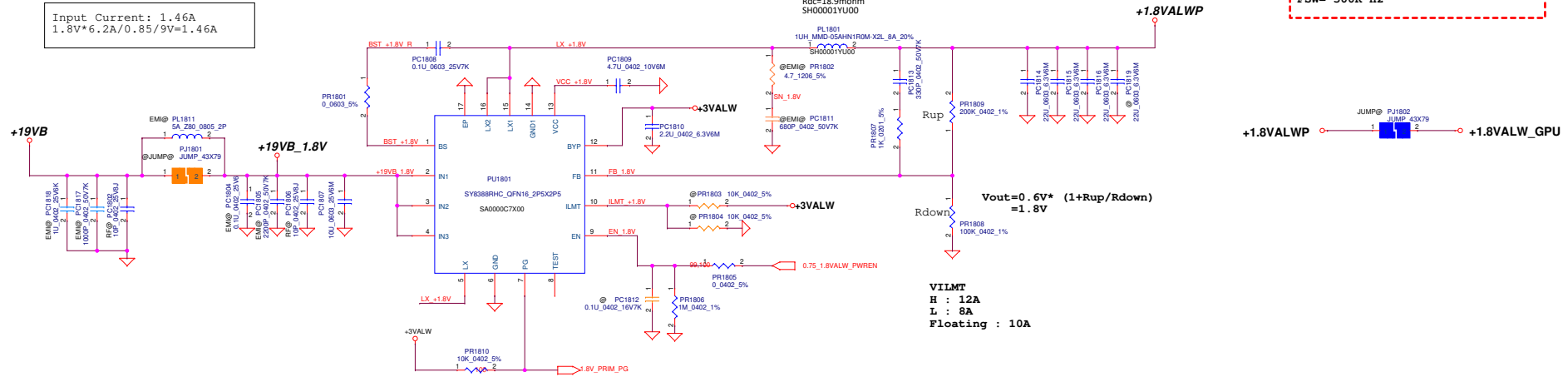
+2.5V_MEM
 Vout= 2.52 V
 TDC 0.203A
 Peak Current 0.29 A
 Current limit 3.6A

Note:
 When design Vin=5V, please stuff snubber
 to prevent Vin damage

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Issued Date	2020/03/05	Deciphered Date	2018/12/31	Title	PWR 1.2VP/0.6VSP+2.5V	
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				Date	Wednesday, April 21, 2021	Rev 0.1
				Sheet	89	of 121

Main Func = 1.8VALWP

Input Current: 1.46A
 $1.8V \times 6.2A / 0.85 / 9V = 1.46A$



```
+1.8VALW_GPU
TDC 5.1A
Peak Current 7.2A
Current limit 10A
OVP=2.106V~2.214V(117%~123%)
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz
```

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				Date	Wednesday, April 14, 2021
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				Date:	Wednesday, April 21, 2021
				Sheet	91 of 121
				Rev	0.1

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Issued Date	2020/03/05	Deciphered Date	2021/08/01	Title	PWR-+VCCIOP
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				Sheet	92 of 121
				Rev	0.1

Reserve for PWR

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Reserve for PWR

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				LA-K453P	0.1	
Date: Wednesday, April 21, 2021				Sheet	94	of 121

Reserve for PWR

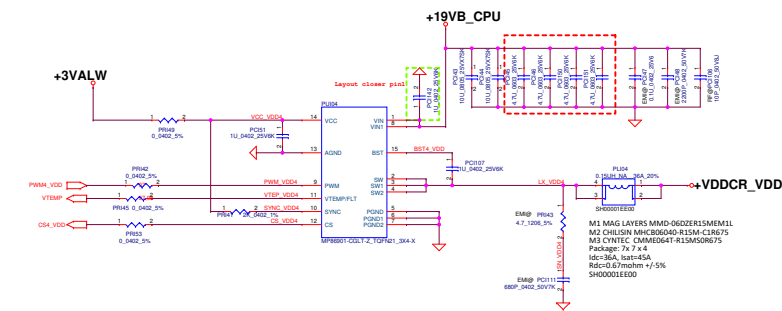
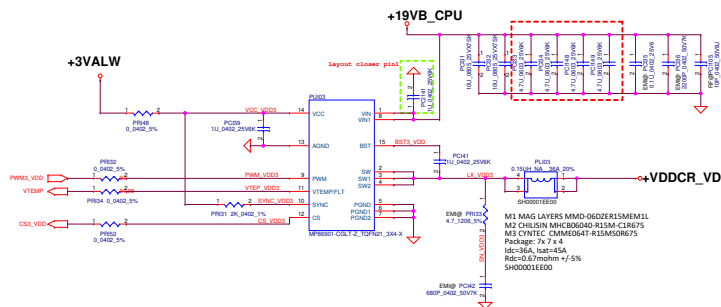
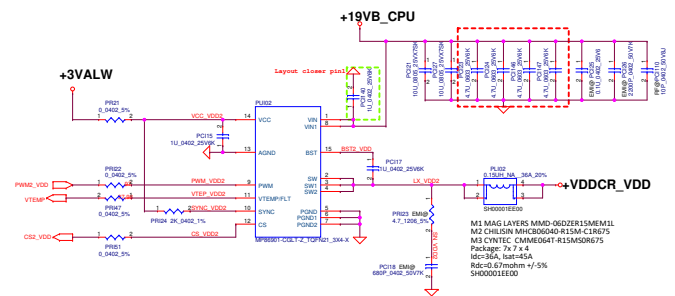
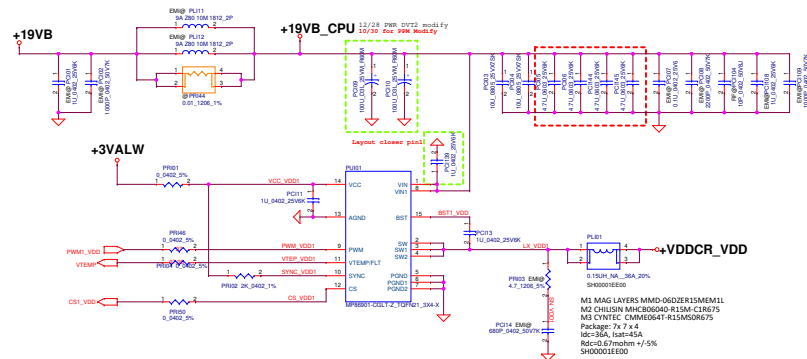
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR	
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				LA-K453P	0.1	
Date: Wednesday, April 21, 2021				Sheet	95	of 121

Reserve for PWR

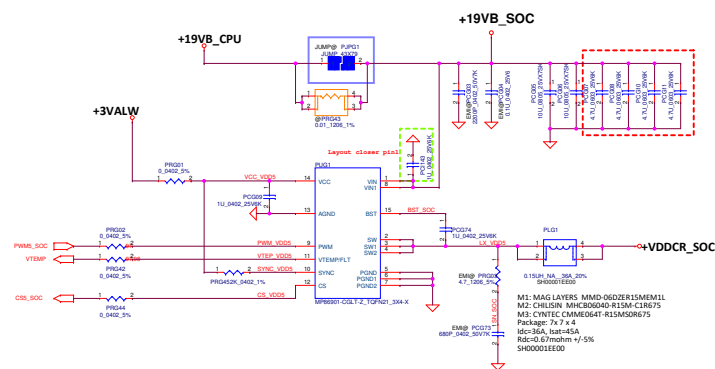
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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR
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Main Func = CPU_CORE_SW

```
+VDDCR_VDD
TDC= 58A
EDP= Peak Current 110A
Loadline 1.1mV/A
```



```
+VDDCR_SOC
TDC= 15 A
EDP= Peak Current 20 A
Loadline 2.7mV/A
```



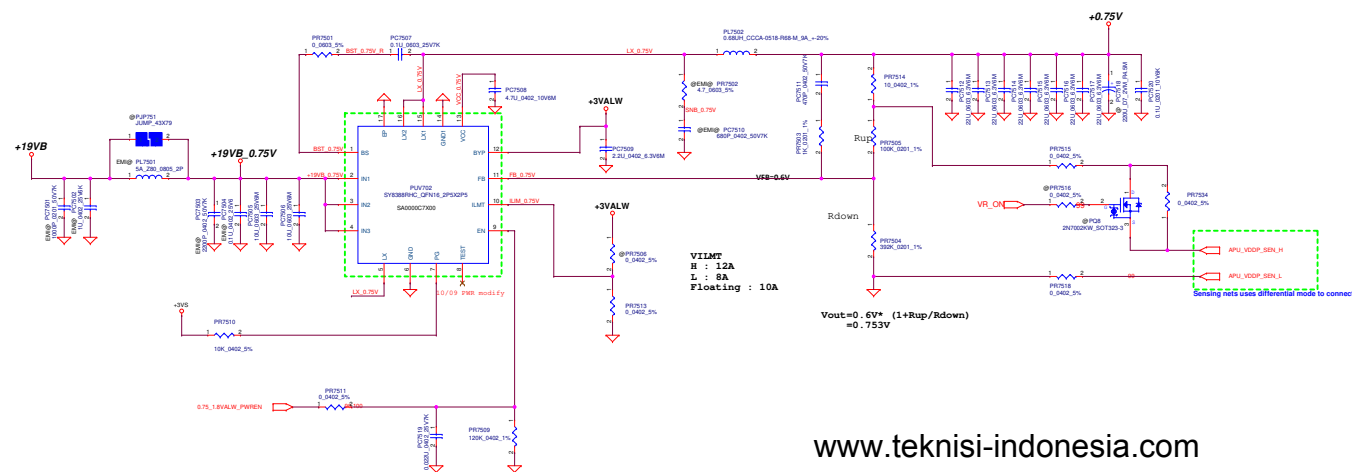
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Issued Date	2020/03/05	Deciphered Date	
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0.75VALW _Input Current : 0.19A
Input Current = 0.753V*2A/0.85/9V=0.19A

```
[SGY]
+VDDP
470uF_ D2 x1
22uF_0603 X 6
0.1uF_0201 x1
```

```
+0.75VALW
Vout = 0.753V
TDC = 2A

OCP current = 8A
OVP = 0.904V (120% Type)
UVP = 0.452V (60% Type)
Fsw = 500KHz
Delta IL = 1.44A
```

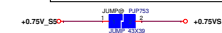


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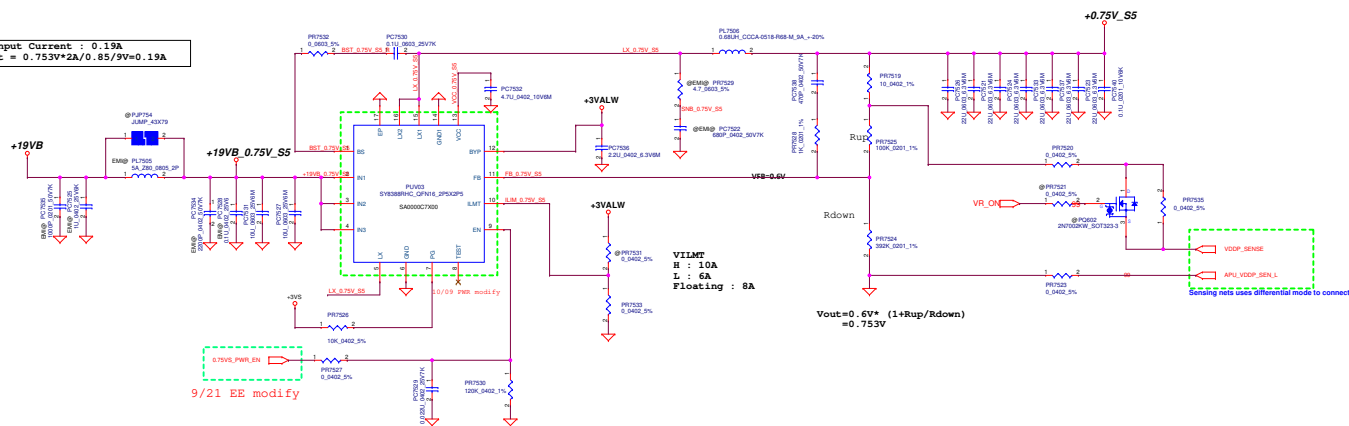
```
[SGY]
+VDDP
470uF_ D2 x1
22uF_0603 X 6
0.1uF 0201 x1
```


```
+0.75VS
Vout = 0.753V
TDC = 2A

OCP current = 8A
OVP = 0.904V (120% Type)
UVP = 0.452V (60% Type)
Fsw = 500KHz
Delta IL = 1.44A
```



+0.75VALW _Input Current : 0.19A
Input Current = $0.753V \cdot 2A / 0.85 / 9V = 0.19A$

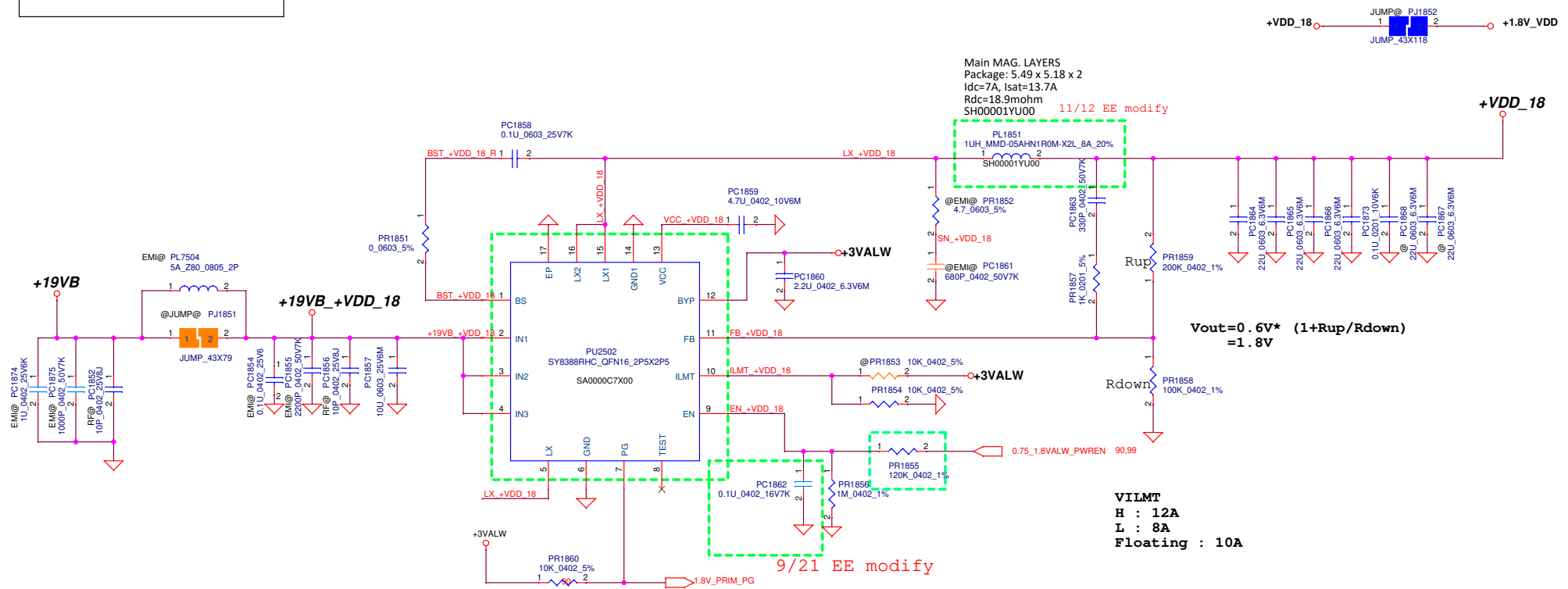


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Date 03/05/2021			Sheet 98 of 101	

Input Current: 0.82A
 $1.8V \times 3.5A / 0.85 / 9V = 0.82A$

```
[SGY]
+VDD_18
470uF_ D2 x1
22uF_0603 X 5
0.1uF_ 0201x1
```

```
+1.8V_VDD
TDC 1.5A
Current limit 8A
OVP=2.106V~2.214V(117%~123%)
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz
```

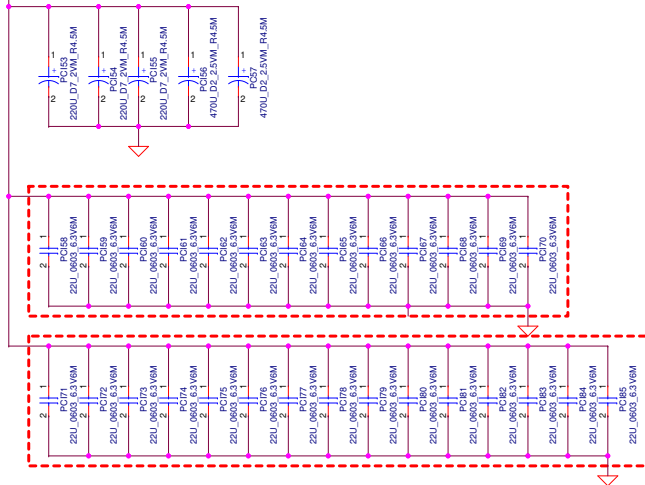


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				LA-K454P	0.1
Date: Wednesday, April 21, 2021				Sheet	100 of 121

[AMD]:
+VDDCR_VDD
22uF_0603 X 16

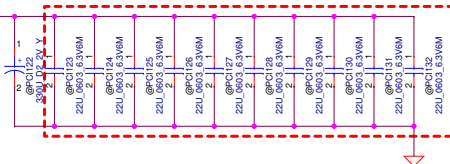
[MPS]
+VDDCR_VDD
470u_D7 x2
220uF_D2 x3
22uF_0603 X 28

+VDDCR_VDD



reserve:
+VDDCR_VDD
330uF_D2 x1
22uF_0603 X 10

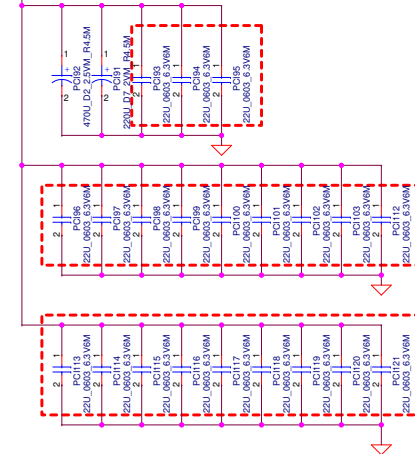
+VDDCR_VDD



[AMD]:
+VDDCR_VDD
22uF_0603 X 7

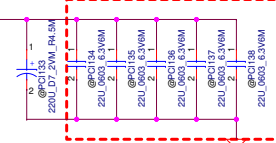
[MPS]
+VDDCR_SOC
470uF_D2 x1
220uF_D2 x1
22uF_0603 X 21

+VDDCR_SOC



resreve:
+VDDCR_SOC
220uF_D7 x1
22uF_0603 X 5

+VDDCR_SOC



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				Sheet	101 of 121

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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR	
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				Date:	Wednesday, April 21, 2021	Sheet 102 of 121

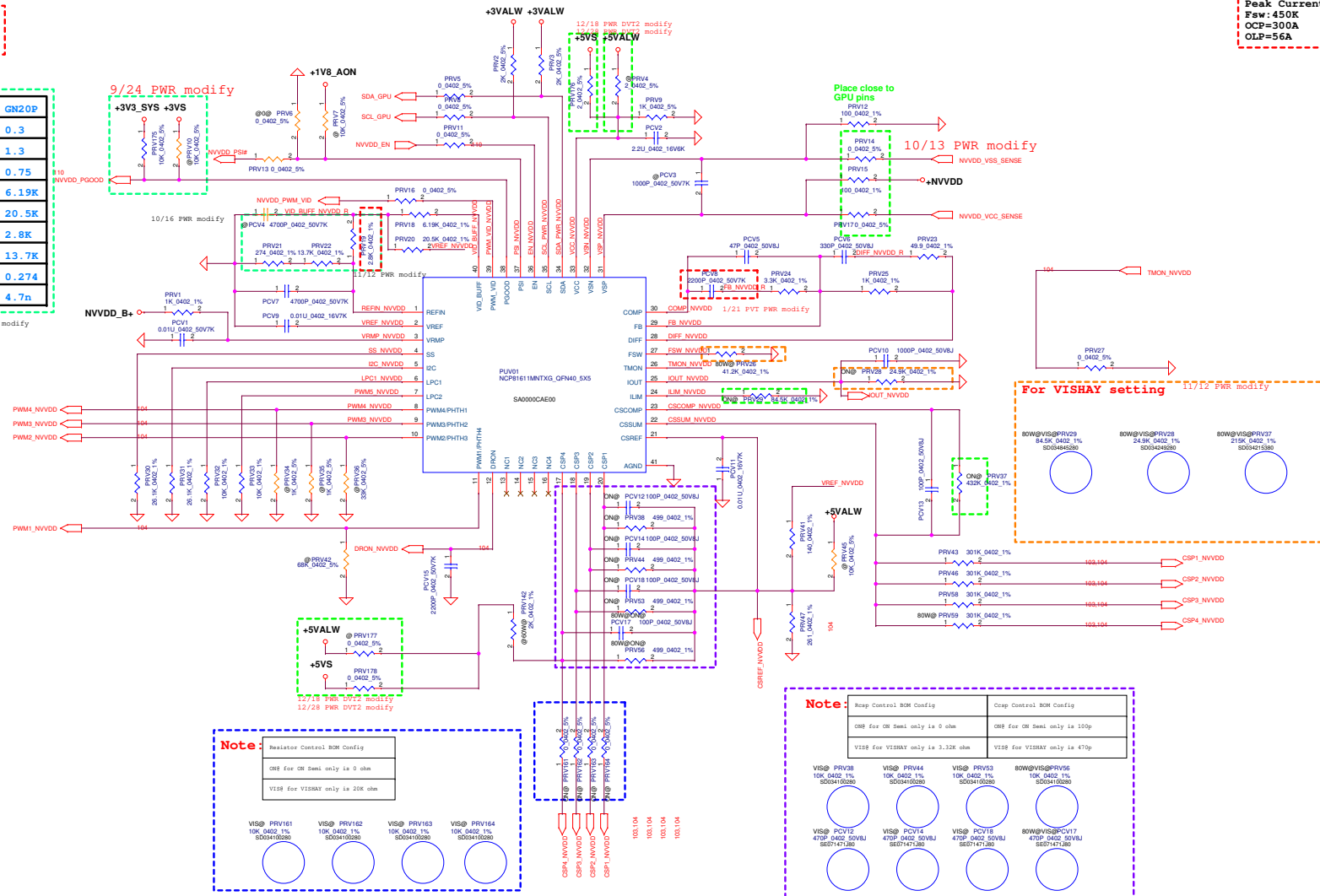
NVVDD
Input Current: $1.2 \times 68 / 0.87 / 12 = 7.8A$

```

NVVDD
TGP 80W
EDPc 68A
Peak Current 225A
Fsw:450K
OCP=300A
OLP=56A

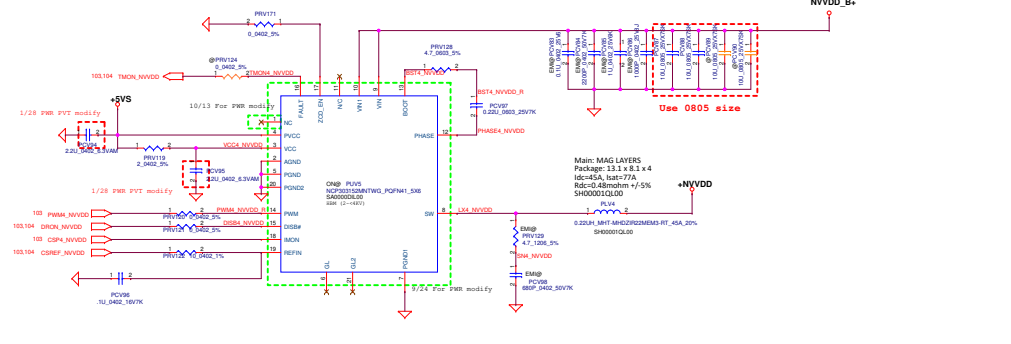
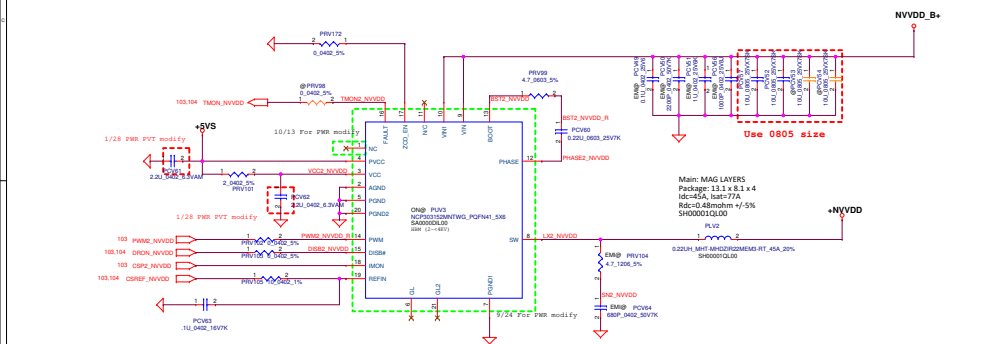
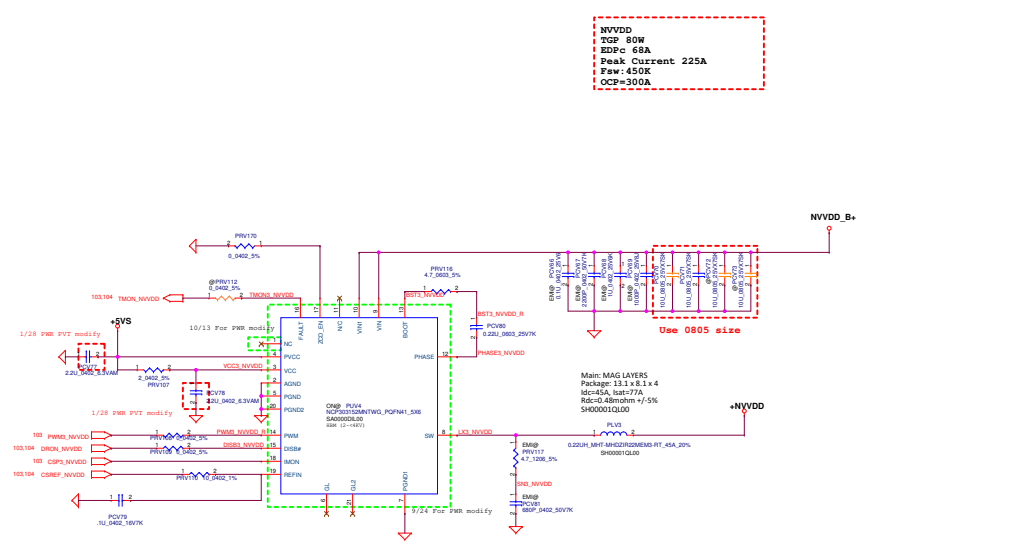
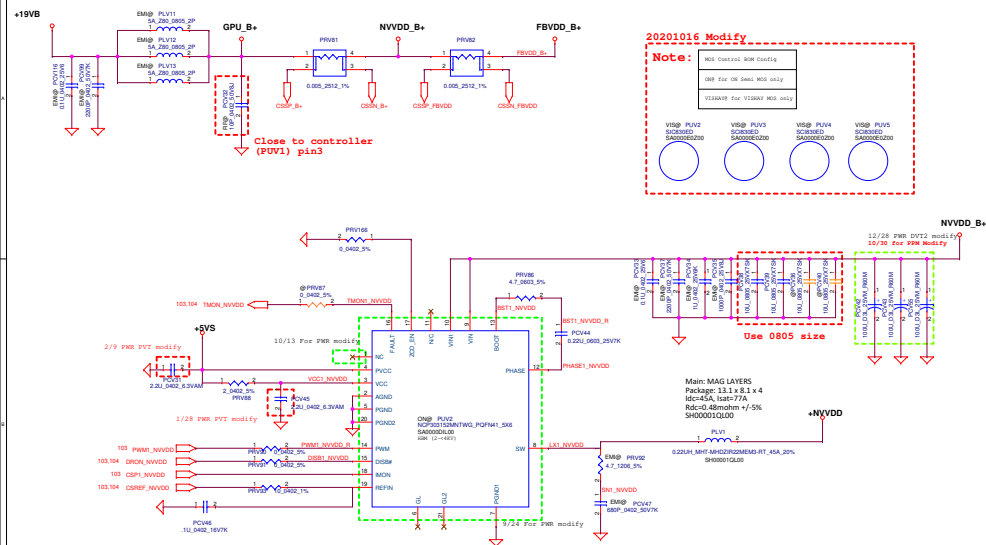
```

Config	GN20P
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	0.274
C	4.7n



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	20200305	Deciphered Date	20200419	File
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Main Func = GPU_CORE SW(1-4PH)



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Issued Date	2020/03/06	Deciphered Date	2020/04/19	File	PWR_YGA_NCP3031S
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LA-K454P					

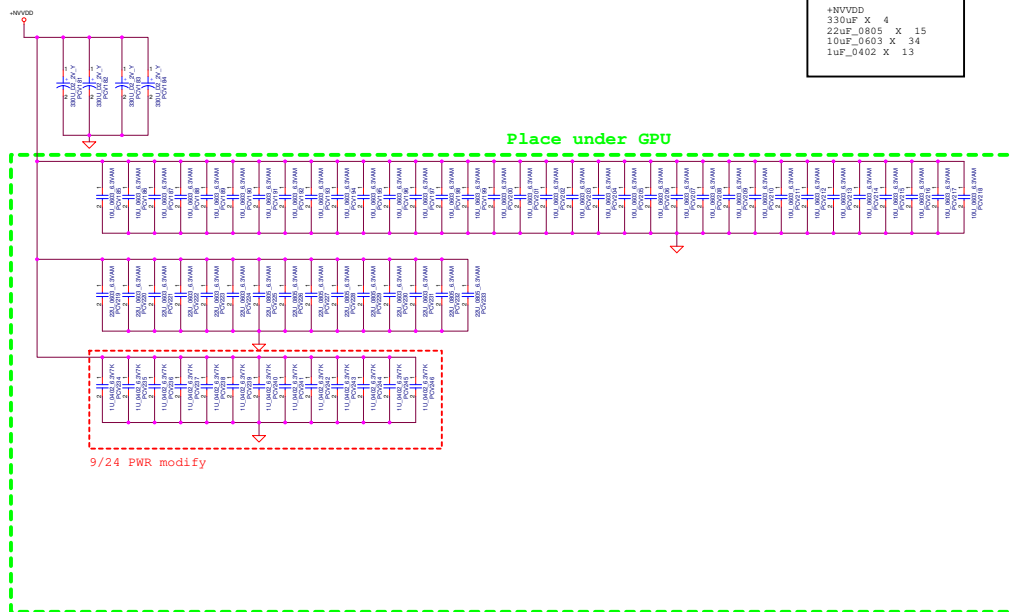
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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	PWR- Reserve for PWR
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				LA-K453P	0.1
				Date: Wednesday, April 21, 2021	Sheet 105 of 121

Reserve for PWR

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Date: Wednesday, April 21, 2021				Sheet	106	of 121

Main Func = VGA CORE DECOUPLING



```
+NVVDD
330uF X 4
22uF_0805 X 15
10uF_0603 X 34
1uF_0402 X 13
```

Security Classification	Compel Secret Data		Title		Compel Electronics, Inc.	
Issued Date	2019/04/19	Declassified Date	2020/04/19	Doc Number		PWR VCA NCP30315
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Reserve for PWR

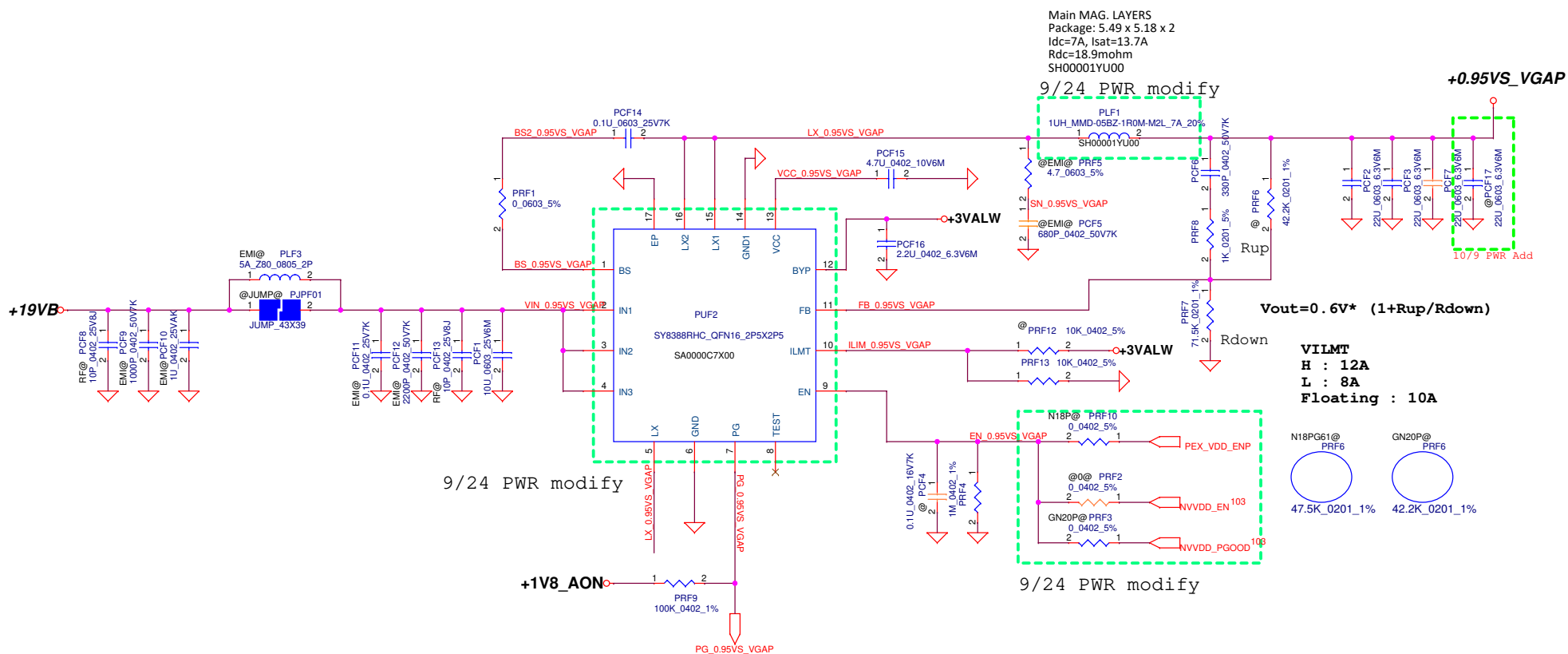
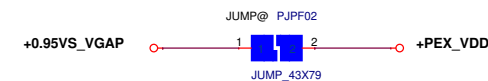
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Main Func =+0.95VS_VGAP

Input Current: 0.974A
 $0.954V \times 2.604A / 0.85 / 3V = 0.974A$

+PEX_VDD	Input Current: $0.95 \times 1.9 / 0.85 / 9 = 0.23$
----------	--

+PEX_VDD
TDC 2.67A
Peak Current 3.82A
OCP Current 8A
Fsw = 500KHz



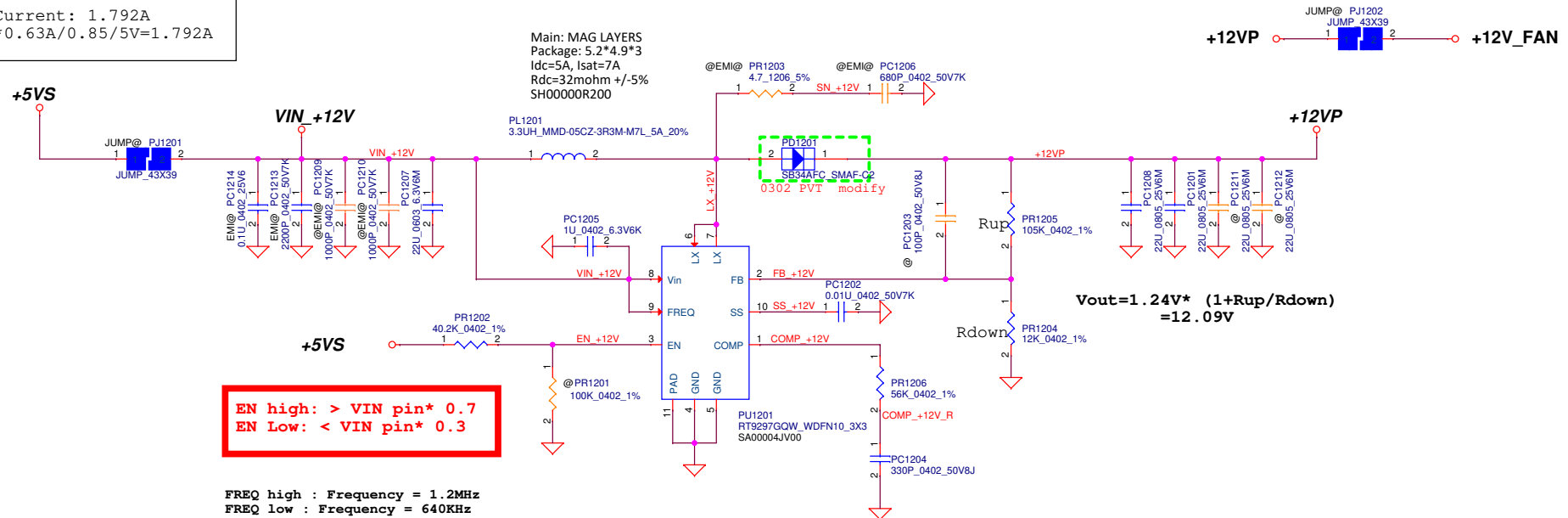
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Main Func =+12VP_FAN

Add a switch circuit to turn off the +12V_VIN if need.

Input Current: 1.792A
 $12.09V \times 0.63A / 0.85 / 5V = 1.792A$

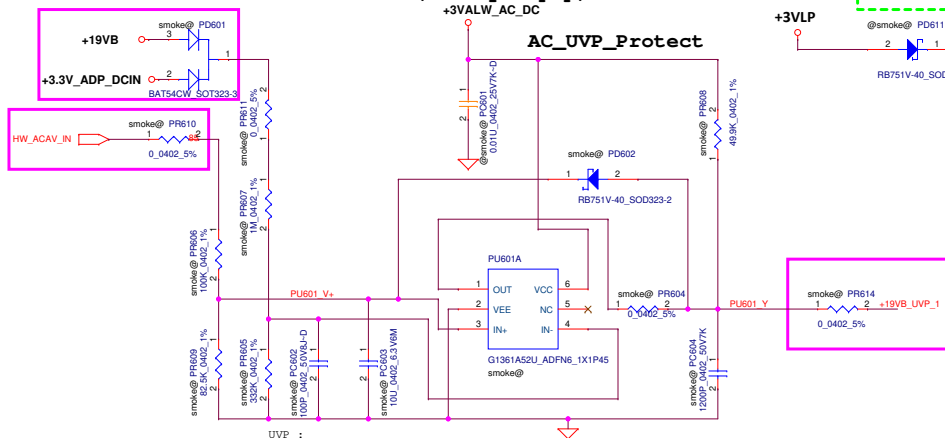
+12V_FAN
Vout = 12.09 V
TDC 0.63A
Peak Current 0.9A
Input Current limit 3A
FSW=1.24MHz



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Main Func = Smokeless UVP

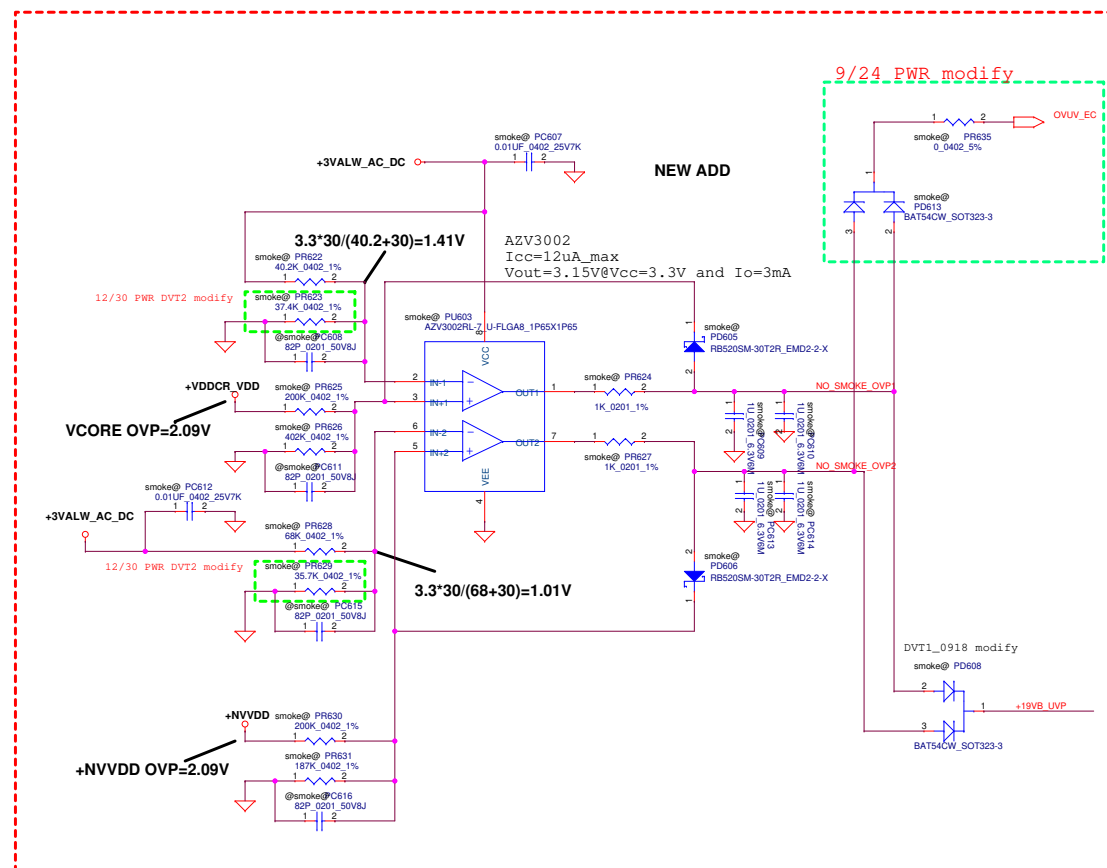
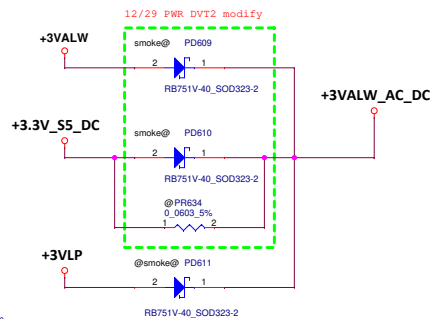
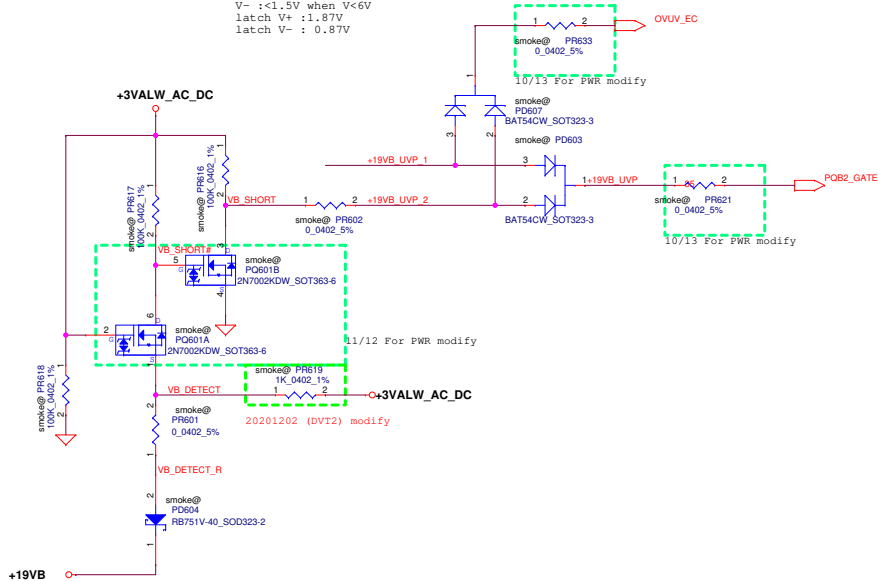
```
AC_UVP_Protect
Barrel disconnct detect (co-lay unpop)
```



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UVP :
PR606 100K
PR609 82.5K
PR607 1M
PR605 332K
PC602 100P
PC603 220P
PR603 1M(depop)
PR604 0
PR608 49.9K
PC604 1200P
V+ : 1.5V
V- : <1.5V when V<6V
latch V+ : 1.87V
latch V- : 0.87V

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Reserve for PWR

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Reserve for PWR

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	97	Vender suggestion is not suitable for additional test points	10/16	PWR	Vender suggestion is not suitable for additional test points,Del	Del PRZ53, PRZ54	X01
2	99	Net Name setting	9/21	EE	EE request naming rule	PUV03 Sequence modify, Net 0.75VS_PWR_EN# change to 0.75VS_PWR_EN	X01
3	100	Sequence modify	9/21	EE	EE request Sequence modify	Sequence modify: Change PR1855 to 120K ohm, Change PC1862 Not loaded	X01
4	107	material shortage	9/24	PWR	BOM change	PCV234-PCV246 Vender Discontinued : Change SE00000WV00 to SE00001EP00	X01
5	110	Solution modify	9/24	PWR	BOM change	Solution modify:Change PUF2 to SY8388, Change PLF1 to SH00001YU00	X01
6	112	Reservation software notification behavior	9/24	PWR	reserve schematic	Add PD613 BAT54CW_SOT323-3, Add PR635 0 ohm	X01
7	103	Sequence modify	9/24	EE	EE request Sequence modify	sequence modify:Change +3VALW to '+3VS, Add PRV175, '+3VS_SYS	X01
8	110	GN20P request	9/24	EE	EE request Sequence modify	PRF10 BOM structure change N18P@;APRF3 BOM structure change GN20P@	X01
9	85	material shortage	10/28	PWR	PPM inform main source(SB00001PI00) shortage_2nd source change to main	SB00001PI00-EE, PQB5 change SB00001PI00 to SB000011K00	X01
10	99	Solution modify	10/09	PWR	BOM change	All planform Unite, PUV702,PUV03 change SA0000C7S00 to SA0000C7X00	X01
11	110	Solution modify	10/09	PWR	Follow SY8388 solution	Follow SY8388 solution, Add PCF17 SE00000M000	X01
12	85	Vendor suggestion	10/11	PWR	BOM change	For Vendor suggestion. PCB17 change SE00000HQ00 to SE000005Z80	X01
13	108	Sequence modify	10/12	EE	EE request Sequence modify	PRW4 change to SD034470180	X01
14	104	vendor request	10/13	PWR	PUV2~PUV5 pin1 NC	PUV2~PUV5 pin1 NC	X01
15	89	Double pulse	10/13	PWR	Vender suggestion. Change lower FW	Vender suggestion. PRM7 Change lower FW	X01
16	112	Reservation software notification behavior	10/13	PWR	PR621,PR635,PR633 POP	PR621,PR635,PR633 POP	X01
17	104	BOM change	9/24	PWR	BOM change	PUV2~PUV5 change toNCP303152	X01
18	82	Net Name modify	10/22	EE	EE request Sequence modify	Net:~+3.3V_ADAP_DCIN change to +3VLP	X01
19	85	Adaptor CP setting	10/28	PWR	BOM change	vendor request PRB16 change from 75K_0402_1% (SD034750280) to 200K_0402_1%(SD034200380)	X01
20	98,104	material shortage	10/30	PWR	PPM inform main/2nd source(SGA0000E000/SGA0000C300) shortage_ new add SGA0000EP00 to main	PPM inform main/2nd source(SGA0000E000/SGA0000C300) shortage_ new add SGA0000EP00 to main	X01
21	103	Increase accuracy	10/13	PWR	For PWR request	Increase accuracy	X01
22	85	reduce inrush	10/30	PWR	BOM change	reduce inrush, PCB12 change to 0.022U	X01
23	103	GPU +NVVDD VBOOT setting	10/16	PWR	BOM change	Vboot*ý-È-×\$ì, PRV19 change to 2.8K ohm, PRV21 change to 274 ohm PRV22 change to 13.7K ohm	X01
24	86	loading=0=j;OSShutdown	9/29	PWR	BOM change	Vboot*ý-È-×\$ì, PRV19 change to 2.8K ohm, PRV21 change to 274 ohm PRV22 change to 13.7K ohm	X01
25	82	Smokeless funtion	9/29	PWR	Stencil Memo modify	PJP601 unmount change mount	X01
26	85	2nd source incomplete replacement	11/12	PWR	BOM change	PDB2 SCS00008E00 change SCS00001200	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	85	Charger B2B MOS 2nd source Bom control setting	10/12	PWR	BOM change	PQB11, PQB12, PQB13, PQB14 add 2nd source SB00001IC00	X01
28	89	2nd source incomplete replacement	10/13	PWR	BOM change	PLM1 SH000000M00 change SH00000PJ00	X01
29	100	Solution modify	11/12	PWR	BOM change	PL1851 SH000014W00 change SH00001YU00	X01
30	103	GPU 2nd source Bom control setting	11/12	PWR	BOM control	PRV29, PRV28, PRV37	X01
31	103	GPU 2nd source Bom control setting	11/12	PWR	BOM control	PRV38, PRV44, PRV53, PRV56 add 2nd source SD034100280 PCV12, PCV14, PCV17, PCV18 add 2nd source SE071471J80 PRV161, PRV162, PRV163, PRV164 add 2nd source SD034100280	X01
32	104	GPU +NVVDD Dr.MOS 2nd source Bom control setting	10/16	PWR	BOM control	PUV2~PUV5 add 2nd source SA0000E0Z00	X01
33	108	material shortage	10/13	PWR	BOM change	PCW42 change to 0.22U	X01
34	112	2nd source incomplete replacement	11/12	PWR	BOM change	Follow 2nd list, PQ601B, PQ601A SB00000PV00 change SB00000E000	X01
35	100	Solution modify	11/12	PWR	BOM change	Solution modify: Change PU2502 to SY8388, Change PL1851 to SH00001YU00	X01
36	85	PWR_CHARGER (ISL95522A)	11/30	PWR	Corrosion issues	PLB11 change from SH00000YE00 to SH00000PJ00	X02
37	87	PWR_+3VALWP/+5VALWP	11/30	PWR	Corrosion issues	PL501 change from SH00001ST00 to SH00001TW00	X02
38	103	PWR_GPU_CORE IC	11/30	PWR	GPU +NVVDD VBOOT setting	1.PRV19 change SD00000J280 to SD034280180 2.PRV22 change SD034165280 to SD034137280. 2.PR21 change SD000017700 to SD034274080.	X02
39	82	PWR_DCIN / BATT CONN / OTP	12/02	PWR	Flashing yellow light issue	1.PR12 change SD000011M00 to SD034100480 2.PR40 change SD043100180 to SD043000080	X02
40	112	PWR_Smokeless UVP/OVP	12/02	PWR	pre charge time	PR619 change SD034100280 to SD034100180	X02
41	108	PWR_GPU_VRAM	12/18	PWR	Materials EOL	PQW2 change from SB00000E000 to SB00001FN00	X02
42	108	PWR_GPU_VRAM	12/18	PWR	1w~dPull high to +5VS power consumption	resever PRW57,PRW180,PRW181	X02
43	103	PWR_GPU_CORE IC	12/18	PWR	1w~dPull high to +5VS power consumption	resever PRV176,PRV177,PRV178	X02
44	85	CHARGER (ISL95522A)	12/25	PWR	Over-discharged battery cannot pre-charged	PRB28 mount, PRB29,PCB31 unmount	X02
45	108	PWR_GPU_VRAM	12/28	PWR	4t°Q=Ä°R ³¥[¹¹q@e@ñ¹q@E,û°C=¶¶@60.1-0.4=§¶i, PWM· AY'¹³¼÷· ³y 'risk	PCW42 unmount	X02
46	85	NVVDD	12/28	PWR	vendor suggest IC, Dr.MOS the same power net	PRV176,PRV178 mount, PRV4,PRV177 unmount	X02
47	85	PWR_CPU_CORE_SW PWR_GPU_CORE SW (NCP303152)	12/28	PWR	material shortage	PPM inform SGA0000EP00 shortage_change main/2nd/3rd change SGA0000C300 / SGA0000E000/SGA0000EP00	X02
48	112	PWR_Smokeless UVP/OVP	12/29	PWR	auto shutdown when run AC power cycling with battery	PD609,PD610 unmount, PR633 mount PR623 change SD034300280 to SD034374280 PR629 change SD034300280 to SD000007D00	X02
49	108	PWR_GPU_VRAM	12/30	PWR	vendor suggest IC, Dr.MOS the same power net	PRW57,PRW181 mount, PRW1,PRW180 unmount	X02
50	85	CHARGER	01/06	PWR	Modify PUB1 For Dell+MYI@E,¹	PUB1(SA0000DTQ10 change SA0000DTQ0L)	A00
51	97	APU	01/06	PWR	material shortage	PCZ1(SE00001R4X0 change SE076103K80)	A00

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